ANALOG DEVICES

Robust, Industrial, Low Power 10BASE-T1L Ethernet PHY

Preliminary Technical Data

ADIN1100

FEATURES

10BASE-T1L IEEE® Std 802.3cg-2019™ compliant
Supports 1.0 V pk-pk & 2.4 V pk-pk transmit levels
Auto-Negotiation capability
Supports intrinsic safety applications
MII & RMII MAC interfaces
MDIO Management Interface, Clause 45 only
Unmanaged configuration using pin strapping including:
- **Master/Slave selection**
- **Transmit amplitude**
- **PHY address**

25 MHz crystal oscillator/25 MHz external clock input (50 MHz external clock for RMII)
Single supply 1.8 V/3.3 V operation (mode dependent)
EMC test standards
- **IEC 61000-4-4 electrical fast transient (EFT) (±4 kV)**
- **IEC 61000-4-2 ESD (±8 kV contact discharge)**
- **IEC 61000-4-2 ESD (±15 kV air discharge)**
- **IEC 61000-4-6 conducted immunity (10 V)**
- **EN55032 radiated emissions (Class A)**

Cable Reach
- **1200 meters+ with 1.0 V pk-pk**
- **1200 meters+ with 2.4 V pk-pk**

Low power consumption
- **Single supply 1 V pk-pk – 45 mW typ**
- **Dual supply 1 V pk-pk – 39 mW typ**
- **Single supply 2.4 V pk-pk – 109 mW typ**
- **Dual supply 2.4 V pk-pk – 81 mW typ**
- **Triple supply 2.4 V pk-pk – 75 mW typ**

3.3 V/2.5 V/1.8 V MAC interface VDDIO supply
Integrated power supply monitoring and POR
Diagnostics
- **Frame Generator and Checker**
- **Multiple Loopback Modes**
- **IEEE Test Mode Support**
- **Cable Diagnostics**

Link/Activity LED
Small package 40-lead (6 mm x 6 mm) LFCSP
Industrial temperature range -40°C to 105°C

APPLICATIONS

Process Control
Factory Automation
Building Automation

GENERAL DESCRIPTION

The ADIN1100 is a low power single port 10BASE-T1L transceiver designed for industrial Ethernet applications and is compliant with the IEEE 802.3cg Ethernet standard for long reach 10 Mb/s Single Pair Ethernet. It integrates an Ethernet PHY core with all the associated analog circuitry, input and output clock buffering, the management interface control register and subsystem registers, as well as the MAC interface and control logic to manage the reset and clock control and pin configuration.

The PHY core supports the 1.0 V pk-pk operating mode and the 2.4 V pk-pk operating mode defined in the standard and can operate from a single power supply rail of 1.8V or 3.3V, with the lower voltage option supporting the 1.0 V pk-pk transmit voltage level.

The 1.0 V pk-pk operating mode, external termination resistors and independent Rx/Tx pins make the ADIN1100 suited to intrinsic safety applications.

The ADIN1100 has an integrated voltage supply monitoring circuit and power on reset circuitry to improve system level robustness.

The MDIO interface is a two-wire serial interface for communication between a host processor or MAC and the ADIN1100, thereby allowing access to control and status information in the PHY core management registers. This interface is compatible with IEEE 802.3 Std Clause 45 management frame structures. The MDIO interfaces of microcontrollers that only support IEEE 802.3 Std Clause 22 cannot be used in their default manner with the ADIN1100 MDIO interface. A common alternative is to use two GPIO pins to replicate the IEEE 802.3 Std Clause 45 frame in software.

The ADIN1100 is available in a 6 mm x 6 mm 40-ld package.

Rev. PrF
Document Feedback

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TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM

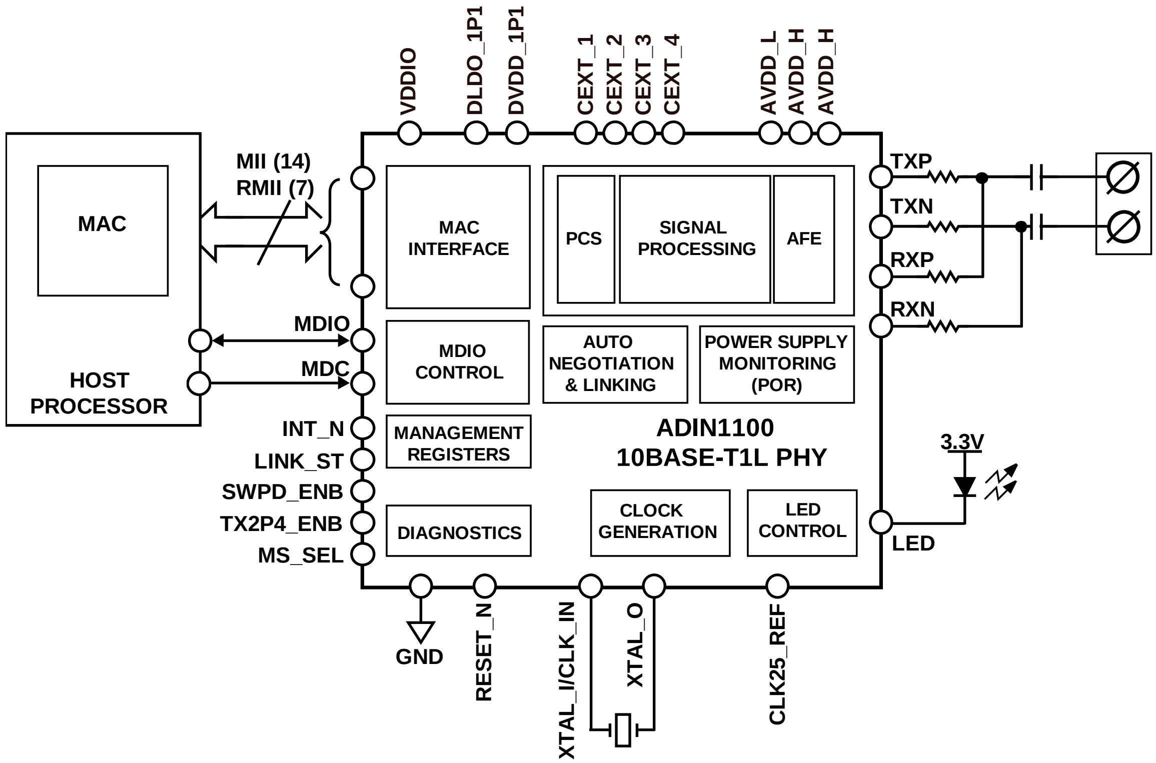


Figure 1.

SPECIFICATIONS

AVDD_H = AVDD_L = VDDIO = 3.3 V; DVDD_1P1 from internal LDO (DVDD_1P1 = DLDO_1P1); All specifications at −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltage Range					
AVDD_H	3.13	3.3	3.46	V	2.4 V pk-pk or 1.0 V pk-pk Transmit Level
AVDD_L	1.71	1.8/3.3	3.46	V	
AVDD_H, AVDD_L	1.71	1.8	3.46	V	1.0 V pk-pk Transmit Level
DVDD_1P1	1.0	1.1	1.2	V	
VDDIO	1.71	1.8/2.5 /3.3	3.46	V	
1.0 V pk-pk Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V DVDD_1P1 = DLDO_1P1
Supply Current, AIDD		25		mA	
Power Consumption		45		mW	100% data throughput, full activity
1.0 V pk-pk Transmit Level (Dual Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V DVDD_1P1 = External 1.1 V
Supply Current, AIDD		16		mA	
Supply Current, DIDD		9		mA	
Power Consumption		39		mW	100% data throughput, full activity
2.4 V pk-pk Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 3.3 V DVDD_1P1 = DLDO_1P1
Supply Current, AIDD		33		mA	
Power Consumption		109		mW	100% data throughput, full activity
2.4 V pk-pk Transmit Level (Dual Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V DVDD_1P1 = DLDO_1P1
Supply Current, AIDD		16.5		mA	
Supply Current, IDDIO		15		mA	
Power Consumption		81		mW	100% data throughput, full activity
2.4 V pk-pk Transmit Level (Triple Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V DVDD_1P1 = External 1.1 V
Supply Current, AIDD		16.5		mA	
Supply Current, IDDIO		6		mA	
Supply Current, DIDD		9		mA	
Power Consumption		75		mW	100% data throughput, full activity
TIMING/LATENCY					
MII Latency					
TX Latency		<3.2		µs	32 bit frames
RX Latency		<6.4		µs	64 bit frames
Total Latency		≤9.6		µs	
DIGITAL INPUTS/OUTPUTS					Applies to MAC interface pins, MDC, MDIO, INT_N, LINK_ST, RESET_N and LED
VDDIO = 3.3 V					
Input Low Voltage (V_{IL})			0.8	V	
Input High Voltage (V_{IH})	2.0			V	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) (min) = 4 mA
Output High Voltage (V_{OH})	2.4			V	Output high current (I_{OH}) (min) = 4 mA
VDDIO = 2.5 V					
V_{IL}			0.7	V	
V_{IH}	1.7			V	
V_{OL}			0.4	V	I_{OL} (min) = 4 mA
V_{OH}	2.0			V	I_{OH} (min) = 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VDDIO = 1.8 V					
V_{IL}			0.3 × VDDIO	V	
V_{IH}	0.7 × VDDIO			V	
V_{OL}			0.2 × VDDIO	V	I_{OL} (min) = 4 mA
V_{OH}	0.8 × VDDIO			V	I_{OH} (min) = 4 mA
RESET_N deglitch time	0.3	0.5	1	μs	
LED OUTPUT					
Output Drive Current	8			mA	VDDIO = 3.3 V
	6			mA	VDDIO = 2.5 V
	4			mA	VDDIO = 1.8 V
CLOCKS					
External Crystal (XTAL)					Requirements for external crystal used on XTAL_I pin and XTAL_O pin
Crystal Frequency		25		MHz	
Crystal Frequency Tolerance	−30		+30	ppm	
Crystal Drive Level		<200		μW	
Crystal ESR			60	Ω	
XTAL_I, XTAL_O $C_{in,eq}$		1.5		pF	Equivalent parallel differential input capacitance looking into XTAL pins
Crystal Load Capacitance (C_L)[1]		10	18	pF	Including PCB trace capacitance and XTAL_I, XTAL_O $C_{in,eq}$
XTAL_I Jitter		2	TBD	ps	Absolute rms jitter, frequency range 1 kHz to 12.5 MHz
Start-up Time			2	ms	Crystal Oscillator Only
Clock Input (CLK_IN)					
Clock Input Frequency		25		MHz	Requirements for external clock applied to XTAL_I pin, MII mode
		50		MHz	RMII mode
Clock Input Voltage Range	0.8		2.5	Vp-p	AC-coupled sine or square wave at XTAL_I pin
Clock Input Duty Cycle	45		55	%	
XTAL_I $Z_{in,eq}$					
R_p		6		kΩ	$R_p \| C_p$
C_p		3		pF	
Jitter			TBD	ps rms	
CLK25_REF clock output					
CLK25_REF Frequency		25		MHz	
V_{OH}		1.05		V	Load 10pF
V_{OL}		0		V	Load 10pF
CLK25_REF Duty Cycle	45		55	%	Load 10pF

[1] Where load capacitance (C_L) = ((C1 × C2)/(C1 + C2) + C_{STRAY}), where C_{STRAY} is the stray capacitance including routing and package parasitics.

TIMING CHARACTERISTICS

POWER-UP TIMING

Table 2. Power Up Timing

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramp time			40	ms
t1	Minimum time interval to internal power good[1]	20		43	ms
t2	Hardware configuration latch time	6	8	14	µs
t3	Management interface active			50	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

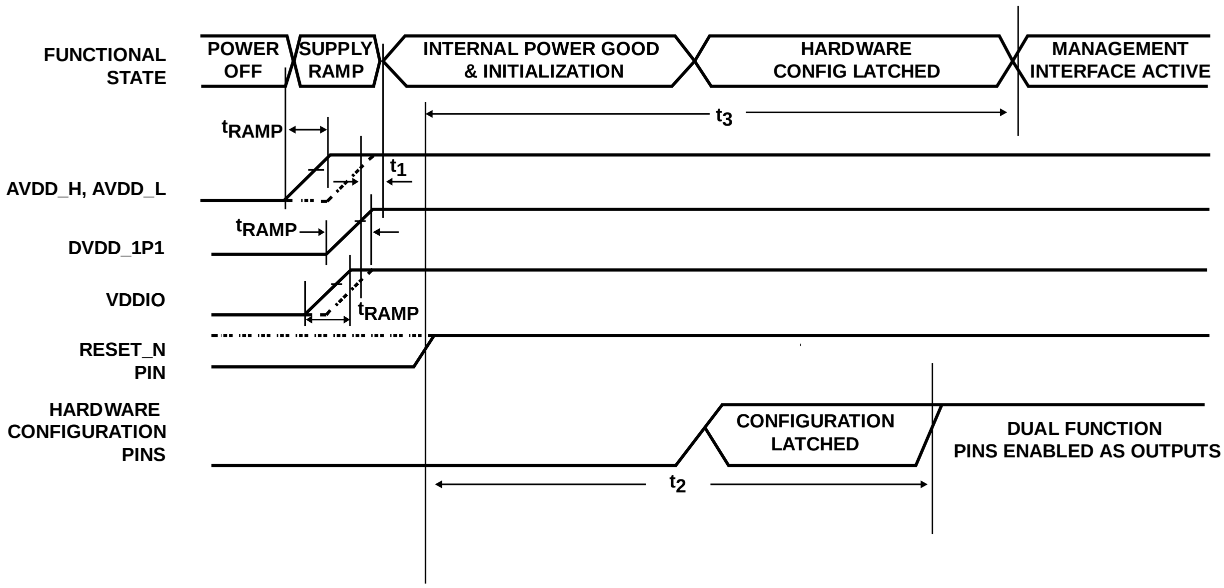


Figure 2. Power-Up Timing

MANAGEMENT INTERFACE TIMING

Table 3. Management Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t1	MDC period	400			ns
t2	MDC high time	100			ns
t3	MDC low time	100			ns
t4	MDC rise/fall time			5	ns
t5	MDIO signal setup time to MDC	10			ns
t6	MDIO signal hold time to MDC	10			ns
t7	MDIO delay time to MDC			300	ns

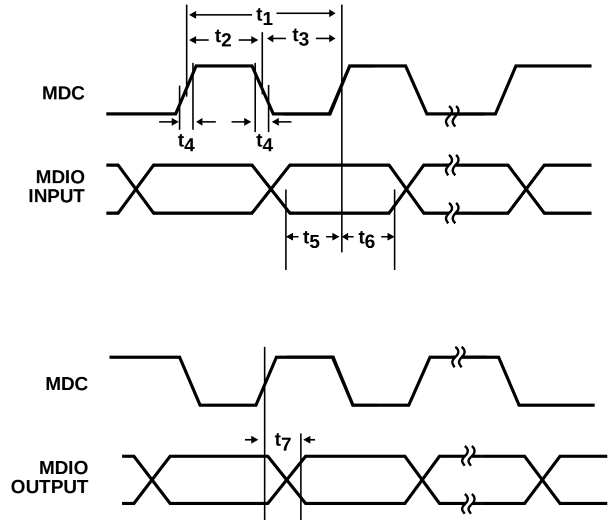


Figure 3. Management Interface Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
VDDIO to GND	−0.3 V to +4 V
DVDD_1P1, DLDO_1P1 to GND	−0.3 V to +1.35 V
AVDD_H, AVDD_L to GND	−0.3 V to +4 V
MAC Interface, MDIO, MDC, INT_N to GND	−0.3 V to VDDIO + 0.3 V
TXN, TXP, RXN, RXP to GND	−0.3 V to AVDD + 0.3 V
LED, RESET_N, LINK_ST to GND	−0.3 V to VDDIO + 0.3 V
XTAL_I/CLK_IN to GND	−0.3 V to 2.75 V
XTAL_O, CLK25_REF to GND	−0.3 V to 1.35 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD	
Human Body Model (HBM)	
TXN, TXP, RXN, RXP Pins	4kV
All Other Pins	2 kV
Machine Model (MM)	200V
Field Induced Charged Device Model (FICDM)	1.25 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

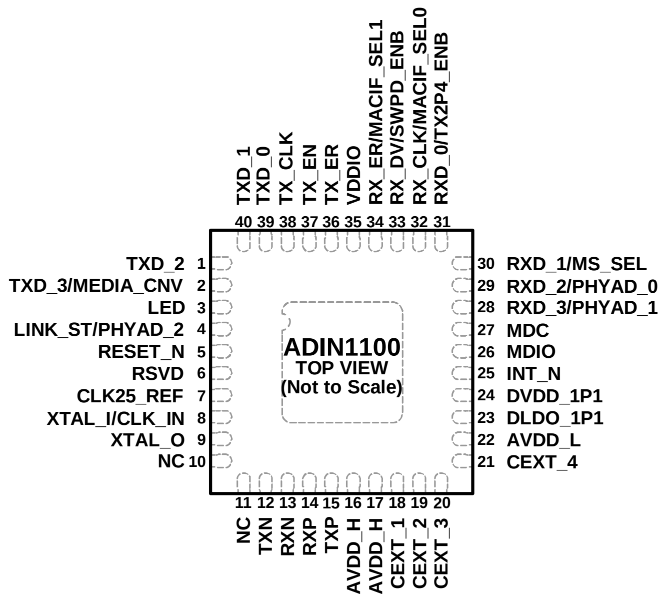
Package Type	θ_{JA}	Unit
CP-40-29	TBD	°C/W

Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS AND TO GND.

Figure 4.

Table 6. Pin Function Descriptions (hardware pin configuration groupings are subject to change)

Pin No.	Mnemonic[1]	Description
CLOCK INTERFACE		
8	XTAL_I/CLK_IN	Input for crystal/single ended 25 MHz reference clock or 50 MHz clock input for RMII.
9	XTAL_O	Crystal output. If using a single ended reference clock on XTAL_I/CLK_IN, leave XTAL_O open circuit. See External Clock Input section.
7	CLK25_REF	Analog reference clock output. The 25 MHz reference clock from the crystal oscillator is available on the CLK25_REF pin. This can be used as an input to another PHY.
MANAGEMENT INTERFACE		
26	MDIO	Management Data Input/Output synchronous to the MDC clock. This pin is open-drain and requires a 1.5 kΩ pull-up resistor to VDDIO.
27	MDC	Management Data Clock input up to 2.5 MHz.
25	INT_N	Management interface interrupt pin output. Open drain, active low output. A low on INT_N indicates an unmasked management interrupt. This pin requires a 1.5 kΩ pull-up resistor to VDDIO.
RESET		
5	RESET_N	Active low input. Hold low for >10 µs. See Hardware Reset section. RESET_N does not require a pull-up resistor as there is an internal pull-up already in place.
MEDIA DEPENDENT INTERFACE (MDI)		
15	TXP	Transmit Positive pin.
12	TXN	Transmit Negative pin.
14	RXP	Receive Positive pin.
13	RXN	Receive Negative pin.
MAC INTERFACE		
28	RXD_3/ PHYAD_1[2]	RXD_3: MII Receive Data 3 output. See the MAC Interface section.
		PHYAD_1: PHY Address hardware configuration pin.

Pin No.	Mnemonic[1]	Description
29	RXD_2/PHYAD_0[2]	RXD_2: MII Receive Data 2 output. See the MAC Interface section.
		PHYAD_0: PHY Address hardware configuration pin.
30	RXD_1/ MS_SEL[2]	RXD_1: RMII/MII Receive Data 1 output. See the MAC Interface section.
		MS_SEL: Master/Slave Selection. Set high for prefer master selection, low for prefer slave selection. See Table 9.
31	RXD_0/TX2P4_ENB[2]	RXD_0: RMII/MII Receive Data 0 output. See the MAC Interface section.
		TX2P4_ENB: Transmit Level Amplitude hardware configuration pin. Set high for 1 V pk-pk transmit amplitude, low supports both 1 V pk-pk and 2.4 V pk-pk transmit amplitude. See Table 10.
32	RX_CLK/MACIF_SEL0[2]	RX_CLK: 2.5 MHz MII Receive Clock output.
		MACIF_SEL0: MAC Interface Selection hardware configuration pin. See Table 11.
33	RX_DV/SWPD_ENB[2]	RX_DV: RMII/MII mode Received Data Valid output. This signal is known as CRS_DV in RMII mode. When asserted high, it indicates valid data is present on the RXD_x pins.
		SWPD_ENB: Software Powerdown Configuration. Set low to configure PHY to enter software powerdown mode after power-up/reset. See Table 8.
34	RX_ER/MACIF_SEL1[2]	RX_ER: RMII/MII mode Receive Error detected output. When asserted high, it indicates that the PHY has detected a receive error.
		MACIF_SEL1: MAC Interface Selection hardware configuration pin. See Table 11.
36	TX_ER	RMII/MII mode Transmit Error detected input from the MAC to the PHY.
37	TX_EN	RMII/MII mode Transmit Enable input from the MAC to the PHY, indicating that transmission data is available on the TXD_x lines.
38	TX_CLK	2.5 MHz MII Transmit Clock output.
2	TXD_3/MEDIA_CNV[2]	TXD_3: MII Transmit Data 3 input. See the MAC Interface section.
		MEDIA_CNV: Media Convertor hardware configuration pin.
1	TXD_2	MII Transmit Data 2 input. See the MAC Interface section.
40	TXD_1	RMII/MII Transmit Data 1 input. See the MAC Interface section.
39	TXD_0	RMII/MII Transmit Data 0 input. See the MAC Interface section.
STATUS		
4	LINK_ST/PHYAD_2[2]	LINK_ST: Link Status output to indicate whether a valid link has been established. LINK_ST is active high.
		PHYAD_2: PHY Address hardware configuration pin.
3	LED	LED: Programmable LED indicator for general purpose LED. The LED is active low. By default, LED is disabled but a common configuration (configured over MDIO) is for the LED to turn on when a link is established and blink when there is activity. See the LED Link/Activity section.
LDO AND REFERENCE DECOUPLING		
18	CEXT_1	External decoupling for reference used in analog circuit. Connect a 4.7 µF cap to ground as close as possible to this pin. When TX2P4_ENB has been set to allow 1 V pk-pk transmission mode only, this capacitor is not required. (See System Level Power Management for more information). Do not use this pin as a voltage source for an external circuit.
19	CEXT_2	External decoupling for LDO circuit. Connect a 0.1 µF cap to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
20	CEXT_3	External decoupling for LDO circuit. Connect a 1 µF cap to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
21	CEXT_4	External decoupling for LDO circuit. Connect a 1 µF cap to ground as close as possible to this pin. When TX2P4_ENB has been set to allow 1 V pk-pk transmission mode only, this capacitor is not required. (See System Level Power Management for more information). Do not use this pin as a voltage source for an external circuit.
POWER AND GROUND PINS		
16, 17	AVDD_H	Analog supply voltage for the various analog circuits in the device. This supply rail can be supplied by 1.8 V to 3.3 V depending on the transmit level configuration. If AVDD_H is 3.3 V both 1.0 V pk-pk and 2.4 V pk-pk transmit operating modes are supported. If AVDD_H is 1.8

Pin No.	Mnemonic[1]	Description
		V only 1.0 V pk-pk transmit operating mode is supported. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
22	AVDD_L	Analog supply voltage for the internal LDOs. This supply rail can be supplied by 1.8 V to 3.3 V. It could be connected direct to the AVDD_H rail in long reach applications or alternatively to the VDDIO rail when the device is configured with dual supplies for lower power consumption. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
35	VDDIO	3.3 V/2.5 V/1.8 V digital power for MDIO and MAC interface. Connect 0.1 µF and 0.01µF capacitors to GND as close as possible to the pin.
24	DVDD_1P1	Input pin for 1.1 V DVDD_1P1 supply rail. When using the internal LDO, connect this pin directly to the DLDO_1P1 pin. Alternatively, an external 1.1 V rail can be provided to the DVDD_1P1 pin for greater power efficiency. Connect a 0.1 µF to ground as close as possible to this pin.
23	DLDO_1P1	Output from an internal 1.1V LDO. This pin can be connected to DVDD_1P1 to eliminate an additional power supply rail. Connect a 0.68 µF cap to ground as close as possible to this pin.
6	RSVD	Reserved. This pin must be connected to GND.
	EP	Exposed Pad. This is GND Paddle and needs to be connected to GND. The LFCSP package has an exposed pad that needs to be connected to GND for electrical reasons and must be soldered to a metal plate on the PCB for mechanical reasons. A 4 × 4 array of thermal vias beneath the exposed GND pad is also recommended.
OTHER PINS		
10, 11	NC	No connect. These pins must be left open-circuit.

[1] Where a pin is shared between a functional signal and a hardware pin configuration, the hardware pin configuration signal is listed last and the pin will be referred to using the functional signal(s) name throughout the datasheet.

[2] All of the hardware configuration pins have internal pull-down resistors. The default mode of operation without any external resistors connected to these pins is captured in Table 7 . If an alternative mode of operation is required, 4.7 kΩ pull-up resistors should be used.

THEORY OF OPERATION

The ADIN1100 is a low power single port 10 Mb/s long reach single pair Ethernet PHY (10BASE-T1L). It is compliant with the IEEE 802.3cg Ethernet standard for long reach 10 Mb/s Single Pair Ethernet.

It integrates a PHY core with all the associated common analog circuitry, input and output clock buffering, the management interface and subsystem registers as well as the MAC interface and control logic to manage the reset and clock control and hardware pin configuration. The ADIN1100 is available in a 40-ld LFCSP package.

POWER SUPPLY DOMAINS

The ADIN1100 has three power supply domains and requires a minimum of one supply rail.

- AVDD_H is the analog power supply input for the analog front end (AFE) circuitry in the ADIN1100.
- AVDD_L is the analog supply voltage for the internal LDOs. It can be connected to the AVDD_H rail when in single supply mode, or to an alternative lower voltage rail when the device is configured with dual supplies for lower power consumption.
- DVDD_1P1 is the 1.1 V digital core power supply input, it can operate from an internal 1.1 V LDO coming from the DLDO_1P1 pin to the DVDD_1P1 pin. Alternatively, it can be driven from an external 1.1 V supply for greater power efficiency.
- VDDIO enables the MDIO and MAC interface voltage supply to be configured independently of the other circuitry on the ADIN1100. It can be connected directly to the AVDD_L rail.

In a single supply application, connect AVDD_H = AVDD_L = VDDIO and use the internal 1.1 V LDO for DVDD_1P1. The appropriate supply voltage used will depend on the end application and cable length. For long reach/trunk applications the higher transmit amplitude of 2.4 V pk-pk requires AVDD_H = 3.3 V whereas spur applications can use a lower transmit amplitude of 1.0 V pk-pk with an AVDD_H = 1.8 V.

MAC INTERFACE

The ADIN1100 provides the option of MII or RMII MAC interfaces. The MAC interface is selected using hardware configuration pins (MACIF_SEL0/1) or via software.

MII Interface Mode

For the RX interface, the ADIN1100 generates a 2.5 MHz RX_CLK signal to synchronize the RXD[3:0] receive data. RX_DV indicates to the MAC that there is valid data present on RXD[3:0]. RX_ER is driven high by the ADIN1100 if an error was detected in the frame that was received from the MDI interface and is being transmitted to the MAC.

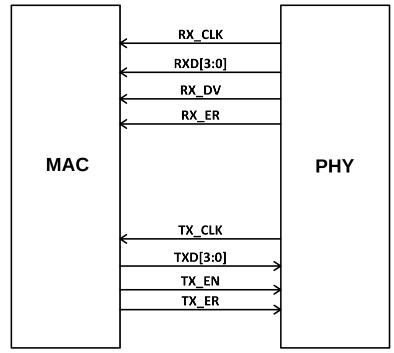


Figure 5. MII MAC-PHY Interface Signals

For the TX interface, the PHY generates a 2.5 MHz reference clock on TX_CLK. The MAC transmits data on TXD[3:0] that is synchronized with TX_CLK. The MAC asserts TX_EN to indicate to the ADIN1100 that transmission data is available on the TXD[3:0] lines.

RMII Interface Mode

RMII mode requires an external 50 MHz clock, which can be sourced from the MAC or an external clock and applied to the XTAL_I/CLK_IN pin for both the TX and RX interfaces. The RMII interface should only be selected from hardware configuration. As RMII mode requires a 50 MHz reference clock, software should not be used to configure the MAC interface to RMII.

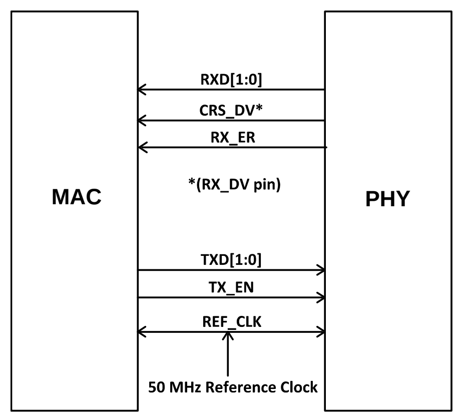


Figure 6. RMII MAC-PHY Interface Signals

The receive data, RXD[1:0], transitions synchronously to the reference clock, REF_CLK. The Carrier sense/Received data valid signal - CRS_DV - is a combination of the CRS and RX_DV signals and is asserted while the receive medium is non-idle. It is asserted asynchronously to REF_CLK and de-asserted synchronously. RX_ER is also synchronous to REF_CLK and asserted when an error is detected in the received frame or when a false carrier is detected. RX_ER assertion on false carrier can be disabled by software.

AUTO-NEGOTIATION

The ADIN1100 uses Auto-Negotiation capability in accordance with IEEE 802.3 Clause 98, providing a mechanism for exchanging information between PHYs to allow link partners to agree to a common mode of operation. During the Auto-Negotiation process, the PHY advertises its own capabilities and compares to those received from the link partner. The concluded operating mode is the transmit amplitude mode and master/slave preference common across the two devices.

In the event of the link being dropped, the Auto-Negotiation process restarts automatically. Auto-Negotiation can be restarted by request through a write to the Auto-Negotiation restart bit (AN_RESTART) in the Auto-Negotiation control register (AN_CONTROL, device address 0x07, register address 0x0200, bit 9).

The Auto-Negotiation process takes some time to complete, depending on the number of pages exchanged, but is always the fastest way to bring up a link. Clause 98 of the IEEE 802.3 standard details the timers related to Auto-Negotiation.

Note, Auto-Negotiation is enabled by default for the ADIN1100 and it is strongly recommended that Auto-Negotiation is always enabled.

Transmit Amplitude Resolution

Auto-Negotiation is used to resolve the transmit amplitude resolution. The PHY can be configured to support both 1.0 V pk-pk and 2.4 V pk-pk transmit levels or to operate with 1.0 V pk-pk transmit level only through the hardware configuration (see Table 10). This configuration can also be done in software using the 10BASE-T1L high level transmit operating mode ability (AN_ADV_B10L_TX_LVL_HI_ABL) and 10BASE-T1L high level transmit operating mode request (AN_ADV_B10L_TX_LVL_HI_REQ) register bits (device address 0x07, register address 0x0204, bits 13 and 12 respectively).

To operate at 2.4 V pk-pk transmit level, both the local and remote PHYs must advertise that they are capable of operating at 2.4 V and at least one PHY must request 2.4 V pk-pk transmit level operation.

If it is required to only operate the PHY at 1.0 V pk-pk transmit level operation, then AN_ADV_B10L_TX_LVL_HI_ABL should be 0, so that 2.4 V pk-pk transmit level operation is not advertised. In this case Auto-Negotiation can only resolve to 1.0 V pk-pk transmit level operation, irrespective of what setting the remote PHY advertises.

Master/Slave Resolution

Auto-Negotiation is also used to resolve master or slave status. The PHY can be configured to prefer slave or prefer master through the hardware configuration (see Table 9). If Auto-Negotiation is disabled, the MS_SEL hardware configuration pin sets the default master/slave selection. Note that the recommended use of the ADIN1100 is with Auto-Negotiation enabled.

During Auto-Negotiation, when prefer slave is selected, and the remote end is prefer or forced Master, the local PHY will be set to slave (and remote to master). When the remote end is prefer or forced slave, the local PHY will be set to master (and remote to slave).

MANAGEMENT INTERFACE

The MII management interface provides a two-wire serial interface between a host processor or MAC and the ADIN1100 allowing access to control and status information in the subsystem and PHY core management registers.

The MII management interface consists of the following:

- MDC, clock line
- MDIO, bidirectional data line
- PHYAD_0, PHYAD_1 and PHYAD_2 pin2 which configure device addresses for each PHY
- INT_N, management interrupt

The interface is compatible with IEEE Standard 802.3 Clause 45 management frame structures (see Register Summary section). Note that the MDIO interfaces of microcontrollers that only support IEEE Standard 802.3 Clause 22 cannot be used to interface with the ADIN1100 MDIO interface. In cases where this is required, the user can replicate the IEEE Standard 802.3 Clause 45 frame using two of the microcontroller's GPIO pins.

Interrupt (INT_N)

The ADIN1100 is capable of generating an interrupt to a host processor or MAC using the INT_N pin in response to a variety of user-selectable conditions. The following conditions can be selected to generate an interrupt:

- Link status change
- MAC interface FIFO overflow/underflow

There is also a non-maskable Hardware reset interrupt. The system interrupt mask and PHY subsystem interrupt mask registers (CRSM_IRQ_MASK and PHY_SUBSYS_IRQ_MASK respectively) are used to make these selections.

When an interrupt occurs, the system can poll the status of the interrupt status register (CRSM_IRQ_STATUS and PHY_SUBSYS_IRQ_STATUS registers) on each device to determine the origin of the interrupt.

MDI INTERFACE

The Media Dependent Interface (MDI) connects the ADIN1100 to the Ethernet network via a twisted wire pair.

The ADIN1100 requires an external hybrid between the separate TXN/P and RXN/P pins and the twisted wire pair. This external hybrid allows the system to have full-duplex communication, by removing the local transmit signal from the combined signal on the cable, leaving just the desired receive signal.

The ADIN1100 hybrid requires a specific topology and values for correct operation. The topology and values for the components can be seen in Figure 7.

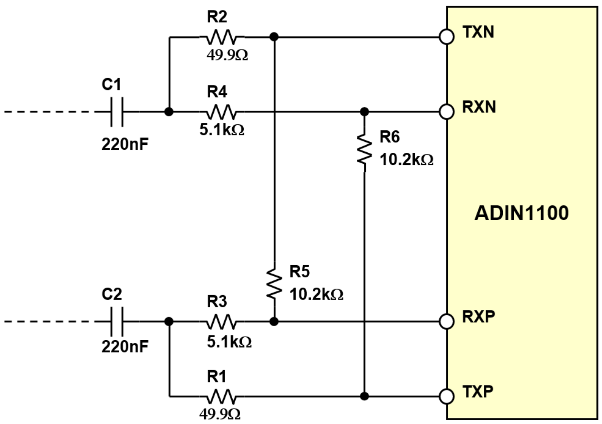


Figure 7. Recommended hybrid for the ADIN1100.

The size, power and voltage rating of these components should be considered in the context of other system requirements, for example, requirements of intrinsic safety.

RESET OPERATION

The ADIN1100 supports a number of resets - power-on reset, hardware reset, and multiple software reset types. All of these put the ADIN1100, including the PHY core into a known state. Whenever the PHY core is reset, the MAC interface output pins (output pins with respect to the ADIN1100) are driven to a low state.

Power-On Reset

The ADIN1100 includes power monitoring circuitry to monitor all of the supplies. At power-up the ADIN1100 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value and the power is considered good.

Brown out protection is provided by monitoring the supplies to detect if one or more of the supplies drops below a minimum falling threshold value and holding the part in hardware reset until the power is good again.

Hardware Reset

A hardware reset is initiated by the power-on reset circuitry or by asserting the RESET_N pin low. The pin should be brought low for a minimum of 10 µs. De-glitch circuitry is included on this pin to reject pulses shorter than approximately 1 µs.

When the RESET_N pin is de-asserted, all the I/O pins are held in tristate mode and the hardware configuration pins are latched, and then the I/O pins are configured for their functional mode. Once all the external and internal supplies are valid and stable, the crystal oscillator circuit is enabled, and after some time for the crystal start-up and stabilization, the PLL is enabled. After approximately 50 ms (max) from the de-assertion of RESET_N, all the internal clocks are valid, the internal logic is released from reset and all the management interface registers are accessible so that the device can be programmed.

Software Reset

A full chip software reset can be initiated by setting the software reset bit (CRSM_SFT_RST, device address 0x1E, register address 0x8810, bit 0). When this bit is set, a full initialization of the chip, almost equivalent to a hardware reset, is done. The I/O pins are held in tristate mode and the hardware configuration pins are latched, and then the I/O pins are configured for their functional mode. The crystal oscillator circuit is enabled, and after some time for the crystal start-up and stabilization, the PLL is enabled. Approximately 10 ms (max) after setting the CRSM_SFT_RST bit, the internal logic is released from reset and all the management interface registers are accessible. The system ready bit (CRSM_SYS_RDY, device address 0x1E, register address 0x8818, bit 0) indicates that the start-up sequence is complete and the system is ready for normal operation.

PHY Subsystem Reset

The PHY subsystem is the part of the ADIN1100 that incorporates the 10BASE-T1L PHY transceiver analog and digital circuits. A PHY subsystem reset can be initiated by setting the PHY subsystem reset register bit (CRSM_PHY_SUBSYS_RST, device address 0x1E, register address 0x8814, bit 0). When this bit is set, the PHY subsystem is reset. The reset is applied for about 1.2 µs and then this bit self clears. All of the PHY digital circuitry is reset and any existing link will drop. The management registers are not initialized by this reset, and access to all the management registers is available during the PHY subsystem reset. This is a short reset and can be used to put the part into a known state while retaining any software initialization of the part.

MAC Interface Reset

A MAC interface reset can be initiated by setting the PHY MAC interface reset register bit (CRSM_MAC_IF_RST, device address 0x1E, register address 0x8815, bit 0). When this bit is set, a reset sequence is provided to the MAC interface to the 10BASE-T1L PHY, but without dropping an existing link. The reset is applied for about 1.2 µs and then this bit self clears. The MAC interface reset will interrupt any TX/RX packet exchange between the MAC and the 10BASE-T1L PHY, but will not drop an existing link, nor will prevent a link being established. No management registers are initialized and access to all the management registers is available during the MAC interface reset.

STATUS LED

LED Link/Activity

The ADIN1100 provides a configurable status LED. The LED can be used to indicate link status and Tx/Rx activity by blinking. By default, the LED is disabled and can be enabled by setting the LED enable bit (LED_EN) within the LED control register (LED_CNTRL, device address 0x1E, register address 0x8C81, bit 0). There is some programmability around the LED on/off blinking activity which is controlled via the LED blink time control register (LED_BLINK_TIME_CNTRL, device address 0x1E, register address 0x8C80).

Link Status Pin

In addition to the LED pin, there is also a LINK_ST pin. This pin is asserted when the link status bit (AN_LINK_STATUS, device address 0x07, register address 0x0201, bit 2) is asserted and indicates that the link is established. The LINK_ST pin is active high.

POWERDOWN MODES

The ADIN1100 supports a number of powerdown modes - hardware powerdown and software powerdown. The lowest power mode is hardware powerdown where the part is turned fully off and the registers are not accessible.

Hardware Powerdown Mode

Hardware powerdown is a useful mode when operation of the ADIN1100 is not required and power is to be minimized. The ADIN1100 enters hardware powerdown mode when the RESET_N pin is asserted and held low. In this mode, all analog and digital circuits are disabled, the clocks are gated off, all the I/O pins are held in tristate mode and the only power is the leakage power of the circuits. The management registers are not accessible in this mode.

Software Powerdown Mode

Software powerdown mode is a useful mode when the part is being configured by software before links are brought up. The ADIN1100 can be configured to enter software powerdown mode after reset using the RX_DV/SWPD_ENB pin. The ADIN1100 can also be instructed to enter software powerdown mode by setting the software powerdown bit (CRSM_SFT_PD, device address 0x1E, register address 0x8812, bit 0).

The software powerdown status bit (CRSM_SFT_PD_RDY, device address 0x1E, register address 0x8818, bit 1) indicates that the part is in the software powerdown state. In software powerdown mode, the analog and digital circuits are in a low power state, the PLL is active and can provide output clocks if configured to do so. Any signal or energy on the MDI pins are ignored and no link will be brought up. The MAC Interface output pins are asserted low. The management interface registers are accessible, and the part can be configured using software. The ADIN1100 exits software powerdown mode when the CRSM_SFT_PD bit is cleared. At this point the PHY will start Auto-Negotiation and attempt to bring up a link after Auto-Negotiation completes successfully.

HARDWARE CONFIGURATION PINS

The ADIN1100 can operate in unmanaged or managed applications. In unmanaged applications, it is possible to configure the desired operation of the PHY from hardware configuration pins without any software intervention. The hardware configuration pins set the default values of the corresponding management registers. After coming out of reset, the PHY will immediately start to attempt to bring up a link. Note for an unmanaged application, the PHY should not be hardware configured to enter software powerdown after reset.

In managed applications, software is available to configure the PHY via the management interface. In this case, the user can configure the PHY to enter software powerdown after reset, software can then intervene to configure the device as required and bring the PHY out of software powerdown to allow links to be established.

Hardware configuration pins are pins shared with functional pins and the voltage level on the pin is sensed and latched upon exiting from a reset. All hardware configuration pins are 2-level sense using a pull-down or pull-up resistor.

HARDWARE CONFIGURATION PIN FUNCTIONS

The following functions are configurable from the ADIN1100 hardware pins:

- PHY address
- Software powerdown mode after reset
- Transmit amplitude configuration
- Master/Slave selection
- MAC interface selection (RMII/MII)
- Media convertor operation.

All of these pins have internal pull-down resistors, so the default mode of operation without any external resistors connected to these pins is captured in Table 7. If an alternative mode of operation is required, 4.7 kΩ pull-up resistors should be used. Note it is only ok to rely on the internal pull-down resistor if the MAC/host also has an internal pull-down on this pin. Otherwise an external pull-down should be used.

Table 7. Default Hardware Configuration Modes

Hardware Configuration Pin Function	Default Mode
PHY address	0x0
Software PD mode after reset	PHY in software PD after reset
Master/slave selection	Prefer slave
Transmit amplitude	1.0 V pk-pk/ 2.4 V pk-pk
MAC interface selection	RMII
Media convertor	Normal PHY operation

PHY Address Configuration

Three of the ADIN1100 pins (RXD_2, RXD_3 and LINK_ST) are available for configuring the PHY address. These are two level configuration pins, which means that it is possible to configure the ADIN1100 to any of the 8 available PHY addresses. In many applications, the default address of 0x0 is used and in that case, it may not be necessary to configure these pins externally because the shared pins have weak internal pull-down resistors. This assumes that no other system level circuitry attached to these nodes, such as the MAC or Ethernet switch has internal pull-up resistors on these pins.

Software Powerdown after Reset

The SWPD_ENB hardware configuration pin is shared with the RX_DV pin and configures the default setting of the software powerdown bit (CRSM_SFT_PD, device address 0x1E, register address 0x8812, bit 0).

If the ADIN1100 is configured so that it does not enter software powerdown mode after reset, then once it exits reset, the ADIN1100 will start Auto-Negotiation and try to bring up a link after Auto-Negotiation completes successfully. If the ADIN1100 is configured so that it enters software powerdown mode after reset, the ADIN1100 will wait in software powerdown mode until it is configured over the MDIO interface at which point, the PHY configuration can be set to exit software powerdown by software.

Table 8. Software Powerdown (Hardware Configuration)

Software Powerdown Configuration	SWPD_ENB
PHY in software PD after reset	0
PHY not in software PD	1

Master/Slave Preference

The MS_SEL hardware configuration pin is shared with the RXD_1 pin and configures the default master/slave selection. If MS_SEL is pulled low during power-up/reset the part is configured by default to prefer slave (this is the case if no external pull-up resistor is connected to MS_SEL pin due to the presence of the internal pull-down resistor). If MS_SEL is pulled high during power-up/reset the part is configured by default to prefer master.

If Auto-Negotiation is disabled, this pin sets the default master/slave selection. Note, Auto-Negotiation is enabled by default for the ADIN1100 and it is strongly recommended that Auto-Negotiation is always enabled.

During Auto-Negotiation when prefer slave is selected, and the remote end is prefer or forced master, the local PHY will be set to slave (and remote to master). When the remote end is prefer or forced slave, the local PHY will be set to master (and remote to slave).

Table 9. Master/Slave Selection (Hardware Configuration)

Master/Slave Selection	MS_SEL
Prefer Slave selection	0
Prefer Master selection	1

The MS_SEL hardware configuration pin configures the default setting of Master/Slave Configuration register bit (AN_ADV_MST, device address 0x07, register address 0x0203, bit 4). The MS_SEL hardware configuration pin also configures the default setting of the master slave config register bit (CFG_MST, device address 0x01, register address 0x0834, bit 14), which is used when Auto-Negotiation is disabled. Note, Auto-Negotiation is enabled by default for the ADIN1100 and it is strongly recommended that Auto-Negotiation is always enabled.

If MS_SEL is pulled low during power-up/reset, the default value of AN_ADV_MST and CFG_MST is 0. If MS_SEL is pulled high during power-up/reset, the default value of these bits is 1.

The AN_ADV_MST bit advertises the master/slave configuration, as follows:

0 = slave;

1 = master.

Transmit Amplitude

The TX2P4_ENB hardware configuration pin is shared with the RXD_0 pin and allows the user to configure the required transmit amplitude mode for the intended application. If TX2P4_ENB is pulled low, the ADIN1100 is configured by default to support both 1.0 V pk-pk and 2.4 V pk-pk transmit levels, to be decided by Auto-Negotiation. If TX2P4_ENB is pulled high, the ADIN1100 is configured to disable 2.4 V pk-pk transmit operating mode by default and operate with 1.0 V pk-pk transmit level only. Note that if the TX2P4_ENB pin is strapped high (1.0 V pk-pk only), the associated register cannot be changed through the MDIO interface, i.e. 2.4 V pk-pk operation is not possible if the ADIN1100 has been hardware pin-configured for 1.0 V pk-pk only.

The 1.0 V pk-pk transmit operating mode supports the spur use case and can operate at a lower AVDD_H supply voltage of 1.8 V. This supports cable lengths of up to 400 m.

The higher transmit operating mode of 2.4 V pk-pk supports trunk applications and requires higher AVDD_H supply voltage (3.3 V). This supports using longer cable lengths of up to 1000 m.

Table 10. Transmit Amplitude Configuration (Hardware Configuration)

Transmit Amplitude Selection	TX2P4_ENB
1.0 V/ 2.4 V pk-pk	0
1.0 V pk-pk	1

The TX2P4_ENB hardware configuration pin configures the value of the 10BASE-T1L high voltage Tx ability read only register bit (B10L_TX_LVL_HI_ABLE, device address 0x01, register address 0x08F7, bit 12). If TX2P4_ENB is pulled low during power-up/reset, the 2.4 V pk-pk transmit operating mode is enabled and the value of B10L_TX_LVL_HI_ABLE is 1. If TX2P4_ENB is pulled high during power-up/reset, the 2.4 V pk-pk transmit operating mode is disabled, and the value of B10L_TX_LVL_HI_ABLE is 0.

The B10L_TX_LVL_HI_ABLE bit reports whether the PHY is capable of operating in the 10BASE-T1L high transmit voltage mode:
0 = PHY does not support 10BASE-T1L high voltage (2.4 V pk-pk) transmit level operating mode;
1 = PHY supports 10BASE-T1L high voltage (2.4 V pk-pk) transmit level operating mode.

The default values of the BASE-T1 Auto-Negotiation advertisement register bits and the 10BASE-T1L transmit voltage amplitude control bit are set to match the 10BASE-T1L high voltage Tx ability bit and it is not possible to write a 1 to these bits if the 10BASE-T1L high voltage Tx ability read only register bit is zero (TX2P4_ENB pin is strapped high i.e. 1.0 V pk-pk only).

The value of the 10BASE-T1L high voltage Tx ability bit configures the default setting of the advertisement of 10BASE-T1L high level transmit operating mode ability bit (AN_ADV_B10L_TX_LVL_HI_ABL, device address 0x07, register address 0x0204, bit 13), the default setting of the advertisement of 10BASE-T1L high level transmit operating mode request bit (AN_ADV_B10L_TX_LVL_HI_REQ, device address 0x07, register address 0x0204, bit 12), and the default setting of the 10BASE-T1L transmit voltage amplitude control bit (B10L_TX_LVL_HI, device address 0x01, register address 0x08F6, bit 12). The latter is used when Auto-Negotiation is disabled. Note, Auto-Negotiation is enabled by default for the ADIN1100 and it is strongly recommended that Auto-Negotiation is always enabled.

- If it is desired to allow both 1.0 V pk-pk and 2.4 V pk-pk transmit level operation then AN_ADV_B10L_TX_LVL_HI_ABL should be set to indicate that the part is capable of 2.4 V pk-pk transmit level operation (and a 3.3V supply is required to power the AVDD_H supply).
- If 2.4 V pk-pk transmit level operation is preferred then AN_ADV_B10L_TX_LVL_HI_REQ should be set, to request 2.4 V pk-pk transmit level operation. Auto-Negotiation will determine the transmit level that the link will operate at.
- If 1.0 V pk-pk transmit level operation is preferred then AN_ADV_B10L_TX_LVL_HI_REQ should be 0. Auto-Negotiation will determine the transmit level that the link will operate at.

To operate at 2.4 V pk-pk transmit level, both the local and remote PHYs must advertise that they are capable of operating at 2.4 V pk-pk and at least one PHY must request 2.4 V pk-pk transmit level operation.

If it is required to only operate the PHY at 1.0 V pk-pk transmit level operation, then the AN_ADV_B10L_TX_LVL_HI_ABL should be 0, so that 2.4 V pk-pk transmit level operation is not advertised. In this case Auto-Negotiation can only resolve to 1.0 V pk-pk transmit level operation, irrespective of what setting the remote PHY advertises. For very long cable lengths depending on the characteristics of the cable it may not be possible to bring up a link at 1.0 V pk-pk operation.

When TX2P4_ENB is 1, the AVDD_H supply can be supplied from either 1.8V or 3.3V for 1.0 V pk-pk transmit level operation.

MAC Interface Selection

The MAC interface hardware configuration pin selection is shared with the RX_CLK and RX_ER pins and can be configured according to Table 11. The RX_CLK and RX_ER pins have weak internal pull-down resistors so, by default the ADIN1100 is configured in RMII mode. External resistors must be used to select the MII MAC interface mode.

Table 11. MAC Interface Selection (Hardware Configuration)

MAC Interface Selection	MACIF_SEL1	MACIF_SEL0
RMII	0	0
Reserved	0	1
Reserved	1	0
MII	1	1

Media Convertor

The ADIN1100 can operate as a media convertor. This allows to have a 10BASE-T PHY connected directly to the ADIN1100 via the RMII interface, connecting to a 10BASE-T1L remote PHY via the MDI pins.

The MEDIA_CNV hardware configuration pin is shared with the TXD_3 pin, therefore, this mode of operation is only available when the RMII MAC interface mode is selected (see Table 11).

The MEDIA_CNV pin has a weak internal pull-down resistor so, by default, the ADIN1100 is configured for normal PHY operation. An external pull-up resistor must be used to select the media convertor operation.

Table 12. Media Convertor Selection (Hardware Configuration)

Media Convertor Selection	MEDIA_CNV
Normal PHY operation	0
Media Convertor operation	1

BRINGING UP 10BASE-T1L LINKS

UNMANAGED PHY OPERATION

For an unmanaged PHY or lightly managed PHY application where there is no software management of the PHY, the hardware configuration pins determine the operating mode. The TX2P4_ENB pin configures the PHY to advertise the support of both 1.0 V pk-pk and 2.4 V pk-pk transmit level operation or to only advertise support of 1.0 V pk-pk transmit level operation. The MS_SEL pin is used to configure the PHY to advertise prefer slave or prefer master. The SWPD_ENB pin should be asserted at power-up and reset so that the PHY does not enter software powerdown mode when it exits reset. Once it exits reset, the ADIN1100 will start Auto-Negotiation and try to bring up a link after Auto-Negotiation completes successfully.

A lightly managed PHY may use the hardware configuration pins to determine the operation of the PHY and to bring up a 10BASE-T1L link. And afterwards software can monitor the operation of the PHY.

MANAGED PHY OPERATION

In a managed PHY application, software is used to configure the PHY operation using the management interface, the hardware configuration pins may be used to set the default values of the registers used to control the transmit amplitude and master/slave setting. The SWPD_ENB pin should be de-asserted at power-up and reset so that the PHY enters software powerdown mode when it exits reset. The PHY will stay in software powerdown mode until the software has configured the PHY and takes it out of software powerdown mode so that it can start Auto-Negotiation and try to bring up a link.

Power-up and Reset Complete

A typical way for software to verify that the part has completed the power-up and reset sequence and is available for normal operation is to read the management register that has the IEEE OUI, model and revision numbers. The value of this register is unique to each PHY vendor and is a non-zero value. If the part has not completed the power-up, the value read will not be correct. In legacy BASE-T PHYs this would be at MI register addresses 2 and 3.

In the ADIN1100 these can also be read at register addresses 2 and 3, but at Clause 45 device address 0x1E. The vendor specific MMD 1 device identifier high register (MMD1_DEV_ID1, device address 0x1E, register address 0x0002, bits [15:0]) has a value of 0x0283 and is the Organizationally Unique Identifier (OUI) bits[3:18]. The vendor specific MMD 1 device identifier low register contains the Organizationally Unique Identifier. bits[19:24] (MMD1_DEV_ID2_OUI, device address 0x1E, register address 0x0003, bits 15:10), the model number (MMD1_MODEL_NUM, bits 9:4) and the revision number (MMD1_REV_NUM, bits 3:0). For the ADIN1100:

- MMD1_DEV_ID1 = 0x0283;
- MMD1_DEV_ID2_OUI = 0x2F
- MMD1_MODEL_NUM = 0x8
- MMD1_REV_NUM = 0x0.

When a valid read of the IEEE OUI is done, the system ready bit (CRSM_SYS_RDY, device address 0x1E, register address 0x8818, bit 0) can also be read to verify that the start-up sequence is complete and the system is ready for normal operation.

The software powerdown status bit (CRSM_SFT_PD_RDY, device address 0x1E, register address 0x8818, bit 1) can be read to check if the part is in the software powerdown state. This is configured by the SWPD_ENB hardware configuration pin.

Configuring the Part for Linking

After power-up or reset, the ADIN1100 should be configured for the desired operation for linking. The ADIN1100 may already be configured as required by the hardware configuration pins, but greater control is available using the management registers.

The Auto-Negotiation process is used to agree the operating mode between a local and remote PHY. For example, Auto-Negotiation is used to agree which PHY operates as master and which as slave and is also used to agree the transmit level.

Auto-Negotiation is enabled by default for the ADIN1100 and it is strongly recommended that Auto-Negotiation is always kept enabled. Auto-Negotiation is defined by the IEEE standard and includes a number of mechanisms to ensure robust linking operation between PHYs and is the fastest way to bring up a link.

Advertisement of Transmit Level Operating Mode

If the 10BASE-T1L high voltage Tx ability read only register bit (B10L_TX_LVL_HI_ABLE, device address 0x01, register address 0x08F7, bit 12) is 1 and there is a 3.3 V supply provided on the AVDD_H pin, the ADIN1100 can support transmit level operation at either 1.0 V pk-pk or 2.4 V pk-pk. The higher transmit level can support longer reach but has high power consumption. The ADIN1100 can support 1.0 V pk-pk transmit level operation with a 1.8 V supply on the AVDD_H pin at very low power consumption. The 1.0 V pk-pk transmit level operation is required for intrinsically safe operation.

The ADIN1100 can either be configured to advertise support of both 1.0 V pk-pk and 2.4 V pk-pk transmit level operation (if B10L_TX_LVL_HI_ABLE = 1) or to advertise support of only 1.0 V pk-pk transmit level operation. This is set using the 10BASE-T1L high level transmit operating mode ability bit within the BASE-T1 Auto-Negotiation advertisement register (AN_ADV_B10L_TX_LVL_HI_ABL, device address 0x07, register address 0x0204, bit 13):
0 = support 1.0 V pk-pk transmit level only;

1 = support both 1.0 V pk-pk and 2.4 V pk-pk transmit level.

The ADIN1100 can also be configured to advertise a request for 2.4 V pk-pk transmit level operation (if B10L_TX_LVL_HI_ABLE = 1). This is set using the 10BASE-T1L high level transmit operating mode request bit (AN_ADV_B10L_TX_LVL_HI_REQ, device address 0x07, register address 0x0204, bit 12):
0 = request 1.0 V pk-pk transmit level;

1 = request 2.4 V pk-pk transmit level.

The link partner advertised transmit level ability can be read in the link partner 10BASE-T1L high level transmit operating mode ability register bit (AN_LP_ADV_B10L_TX_LVL_HI_ABL, device address 0x07, register address 0x0207, bit 13). The link partner advertised transmit level request can be read in the link partner 10BASE-T1L high level transmit operating mode request register bit (AN_LP_ADV_B10L_TX_LVL_HI_REQ, device address 0x07, register address 0x0207, bit 12). These bits are updated during the Auto-Negotiation process and are valid when the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set.

If either the local or remote PHY advertises that it is not capable of transmitting in the high level (2.4 V pk-pk) transmit operating mode or if neither the local nor remote PHY advertises a request for high level (2.4 V pk-pk) transmit operating mode, then the result will be operation at 1.0 V pk-pk transmit level.

If both the local and remote PHY advertises that they are capable of transmitting in the high level (2.4 V pk-pk) transmit operating mode and if either the local or remote PHY advertises a request for high level (2.4 V pk-pk) transmit operating mode, then the result will be operation at 2.4 V pk-pk transmit level.

Hence, a PHY can ensure it must operate at 1.0 V pk-pk transmit level. But it can only request operation at 2.4 V pk-pk transmit level.

Table 13. Determination of Transmit Level by Auto-Negotiation

HI_ABL[1]	HI_REQ[1]	LP_HI_ABL[1]	LP_HI_REQ[1]	Transmit Level
0	X	0	X	1.0 V pk-pk
1	X	0	X	1.0 V pk-pk
0	X	1	X	1.0 V pk-pk
1	0	1	0	1.0 V pk-pk
1	0	1	1	2.4 V pk-pk
1	1	1	0	2.4 V pk-pk
1	1	1	1	2.4 V pk-pk

[1]HI_ABL, HI_REQ, LP_HI_ABL and LP_HI_REQ refer to the advertisement bits AN_LP_ADV_B10L_TX_LVL_HI_ABL, AN_LP_ADV_B10L_TX_LVL_HI_REQ, AN_ADV_B10L_TX_LVL_HI_ABL and AN_ADV_B10L_TX_LVL_HI_REQ respectively.

Advertisement of Master/Slave

The 10BASE-T1L standard uses what is known as a master/slave clock scheme. This is commonly used in full-duplex transceiver standards using echo cancellation. One PHY is designated as the master and the other PHY as the slave. Auto-Negotiation is used to agree which PHY is the master and which is the slave and it generally doesn't matter which is which.

The ADIN1100 has an internal pull-down resistor on the MS_SEL pin and this results in a default setting of configuring the PHY to advertise prefer slave. The recommendation is to either use the default setting of advertise prefer slave or to use a setting of advertise prefer master.

If it is mandatory for the PHY to operate as master, then an advertise forced mater configuration should be used. However, this should be used with caution, as if remote end is also forced master, there is a configuration fault and Auto-Negotiation will fail and the link will not come up.

The force master/slave configuration register bit (AN_ADV_FORCE_MS, device address 0x07, register address 0x0202, bit 12) is used to configure the PHY to advertise its master/slave configuration as a preference or as a forced value, as follows:
0 = master/slave configuration is a preferred mode;
1 = master/slave configuration is a forced mode.

The master/slave configuration register bit (AN_ADV_MST, device address 0x07, register address 0x0203, bit 4) is used to configure the PHY to advertise its master/slave configuration, as follows:
0 = slave;
1 = master.

The link partner advertised master/slave setting can be read in the link partner force master/slave configuration register bit (AN_LP_ADV_FORCE_MS, device address 0x07, register address 0x0205, bit 12) and the link partner master/slave configuration register bit (AN_LP_ADV_MST, device address 0x07, register address 0x0206, bit 4). These bits are updated during the Auto-Negotiation process and are valid when the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set.

When the local and remote PHY have the same preferred configuration, e.g. both slave or both master; a random process is used to determine which is master and which is slave. When one PHY has a forced configuration, its master/slave configuration is given priority over a PHY with a preferred setting where both PHYs have the same master/slave configuration. If both PHYs have a forced configuration and the same master/slave configuration, there is a configuration fault and Auto-Negotiation will fail.

Table 14. Determination of Master/Slave by Auto-Negotiation

Local		Remote		Local	Remote
Force[1]	MST[1]	Force[1]	MST[1]	M/S Resolution	
0	0	0	0	Master/Slave	Slave/Master
0	0	0	1	Slave	Master
0	1	0	0	Master	Slave
0	1	0	1	Master/Slave	Slave/Master
0	X	1	0	Master	Slave
0	X	1	1	Slave	Master
1	0	0	X	Slave	Master
1	1	0	X	Master	Slave
1	0	1	0	Config Fault	Config Fault
1	0	1	1	Slave	Master
1	1	1	0	Master	Slave
1	1	1	1	Config Fault	Config Fault

[1] Where Force and MST refer to the advertisement bits AN_ADV_FORCE_MS, AN_ADV_MST, AN_LP_ADV_FORCE_MS and AN_LP_ADV_MST.

The resolution of master/slave can be read using the master/slave resolution result register bits (AN_MS_CONFIG_RSLTN, device address 0x07, register address 0x8001, bits 6:5). This indicates if the PHY is configured as a slave or a master or if there was a configuration fault. These bits are updated during the Auto-Negotiation process and are valid when the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set.

Successful Completion of Auto-Negotiation

When Auto-Negotiation has completed, the Auto-Negotiation complete indication register bit (AN_LINK_GOOD, device address 0x07, register address 0x8001, bit 0) is set. This bit indicates completion of the Auto-Negotiation transmission, and that the enabled PHY technology is either bringing up its link, or that it has brought up its link.

When Auto-Negotiation has completed and the link is up the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set. When this bit is read as one, it means that the Auto-Negotiation process has been completed, the PHY link is up, and that the contents of the AN_ADV_ABILITY and AN_LP_ADV_ABILITY register bits are valid.

Link Status

The status of the link can be determined by reading the link status register bit (AN_LINK_STATUS, device address 0x07, register address 0x0201, bit 2). This bit latches low. When read as one, this bit indicates that a valid link has been established. If this bit reads zero, it means that the link has failed since the last time it was read. If the value of this bit is read as zero, it needs to be read a second time to determine the link status at this time (see Latch Low Registers section).

In the event of the link being dropped, the Auto-Negotiation process restarts automatically. Auto-Negotiation can be restarted by request through a write to the Auto-Negotiation restart bit (AN_RESTART) in the Auto-Negotiation control register (AN_CONTROL, device address 0x07, register address 0x0200, bit 9).

ON-CHIP DIAGNOSTICS

LOOPBACK MODES

The PHY core provides several loopback modes: PMA loopback, PCS loopback, MAC interface loopback and MAC interface remote loopback. An external MII or RMII loopback can also be configured (see Figure 8). These loopback modes test and verify various functional blocks within the PHY. The use of frame generator and frame checkers allow completely self contained in-circuit testing of the digital and analog data paths within the PHY core.

PMA Loopback

For PMA loopback, leave the MDI pins open-circuit, thereby transmitting into an unterminated connector/cable. For the most accurate results leave the cable disconnected. The PHY can then operate by receiving the reflection from its own transmission. This loopback is intended as an implementation of IEEE Std 802.3cg subclause 146.5.6 PMA Local Loopback. Note that for 10BASE-T1L PMA local loopback, the device needs to be configured in the forced link configuration mode (Auto-Negotiation disabled). Setting the B10L_LB_PMA_LOC_EN bit (B10L_PMA_CNTRL register, device address 0x01, register address 0x08F6) enables PMA loopback.

PCS Loopback

PCS loopback mode loops the Tx data back to the Rx within the PCS block at the input stage of the PHY digital block. Setting the B10L_LB_PCS_EN bit (B10L_PCS_CNTRL register, device address 0x03, register address 0x08E6) enables PCS loopback.

When the PCS loopback mode is enabled, no signal is transmitted to the MDI pins.

MAC Interface Loopback

MAC interface loopback mode loops the data received on the MAC interface TXD pins back to the RXD pins and can therefore be used to verify correct MAC interface connectivity. Setting the MAC_IF_LB_EN bit (MAC_IF_LOOPBACK register, device address 0x1E, register address 0x803D) enables MAC interface loopback. Note that if the MAC_IF_LB_TX_SUP_EN bit, within the same register, is set, which is its default state, then transmission of the signal is suppressed to the MDI pins.

MAC Interface Remote Loopback

MAC interface remote loopback requires a link up with a remote PHY and enables looping of the data received from the remote PHY back to the remote PHY. This linking allows a remote PHY to verify a complete link by ensuring that the PHY receives the proper data. Setting the MAC_IF_REM_LB_EN bit (MAC_IF_LOOPBACK register, device address 0x1E, register address 0x803D) enables MAC interface remote loopback. Note that if the MAC_IF_REM_LB_RX_SUP_EN bit, within the same register, is set, which is its default state, then the data received by the PHY is suppressed and not sent to the MAC.

External MII/RMII Loopback

The final loopback modes highlighted in Figure 8 are the external MII/RMII loopback.

The external MII loopback does not require any particular register bits to be set in order to enable it. It requires the shorting of the RXD_[0:3] pins to the TXD_[0:3] pins as well as RX_DV to TX_EN and RX_ER to TX_ER.

To use the external RMII loopback, it is required to short the pins RXD_[0:1] to the TXD_[0:1] pins as well as the pin CRS_DV to the pin TX_EN. In addition to this, the RMII TXD check enable bitfield (RMII_TXD_CHK_EN, device address 0x1E, register address 0x8038, bit 0) has to be set to 1 so CRS_DV can be connected to TX_EN.

These two modes enable the looping of the data received from the remote PHY back to the remote PHY.

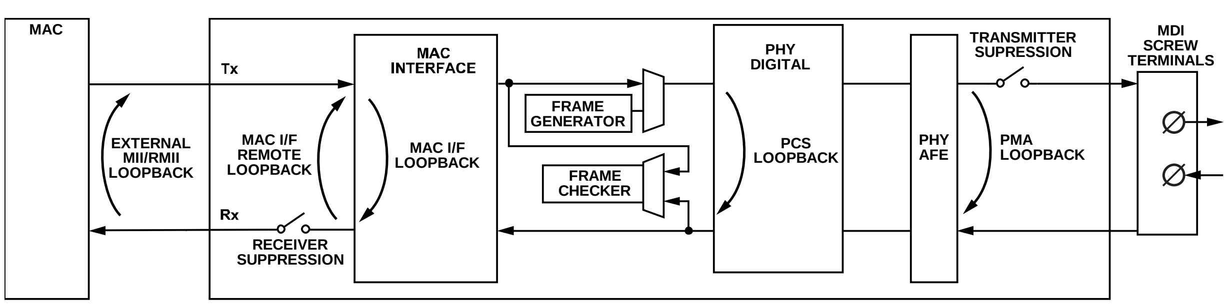


Figure 8. ADIN1100 Loopback Modes

FRAME GENERATOR AND CHECKER

The ADIN1100 can be configured to generate frames and to check received frames (see Figure 9). The frame generator and checker can be used independently to just generate frames or just check frames or can be used together to simultaneously generate frames and check frames. If frames are looped back at the remote end, the frame checker can be used to check frames generated by the ADIN1100.

When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled (CRSM_DIAG_CLK_EN, device address 0x1E, register address 0x882C, bit 0).

The frame generator control registers configure the type of frames to be sent (random data, all 1s, etc.), the frame length, and the number of frames to be generated.

The generation of the requested frames starts by enabling the frame generator (set the FG_EN bit, device address 0x1E, register address 0x8015, bit 0). When the generation of the frames is completed, the frame generator done bit is set (FG_DONE, device address 0x1E, register address 0x801E, bit 0).

The frame checker is enabled using the frame checker enable bit (FC_EN, device address 0x1E, register address 0x8001, bit 0). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY, which is configured using the frame checker transmit select bit (FC_TX_SEL, device address 0x1E, register address 0x8005, bit 0). The frame checker reports the number of frames received, cyclic redundancy check (CRC) errors, and various other frame errors. The frame checker frame counter register and frame checker error counter register count these events.

The frame checker counts the number of CRC errors and these are reported in the receive error counter register (RX_ERR_CNT, device address 0x1E, register address 0x8008). To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched when the receive error counter register is read. Therefore, when using the frame checker, read the receive error counter first, and then read all other frame counters and error counters. A latched copy of the receive frame counter register is available in the FC_FRM_CNT_H register and FC_FRM_CNT_L register (device address 0x1E, register addresses 0x8009 and 0x800A respectively).

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frames errors, and undersized frame errors. In addition to the received frames, the frame checker counts frames with an odd number of nibbles in the frame, and counts packets with an odd number of nibbles in the preamble. The frame checker also counts the number of false carrier events, which is a count of the number of times the bad start of stream delimiter (BAD SSD) state is entered.

Frame Generator and Checker used with Remote Loopback with Two PHYs

Using two PHY devices, the user can configure a convenient self-contained validation of the PHY to PHY connection. Figure 9 shows an overview of how each PHY is configured. An external cable is connected between both devices, and PHY1 is generating frames using the frame generator. PHY2 has MAC interface remote loopback enabled (MAC_IF_REM_LB_EN). The frames issued by PHY1 are sent through the cable, through the PHY2 signal chain returned by PHY2 MAC interface remote loopback, back again through the cable, and checked by the PHY1 frame checker.

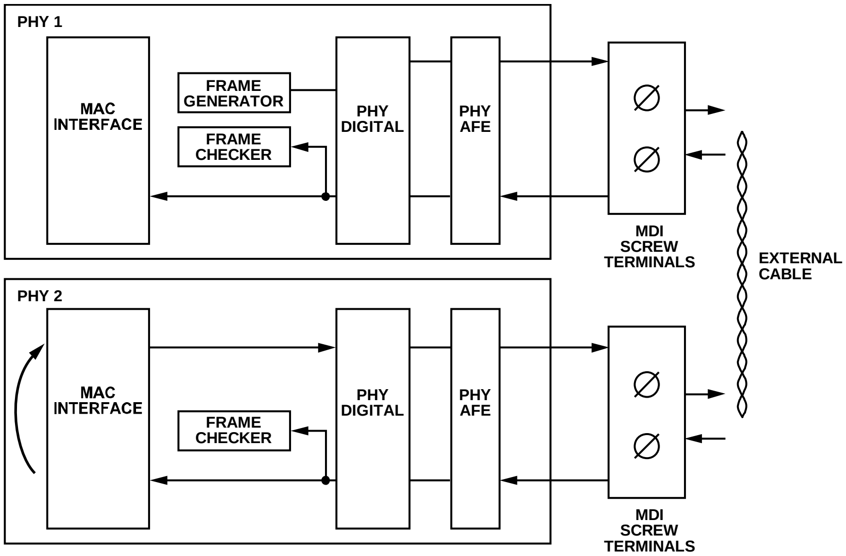


Figure 9. Remote Loopback used across Two PHYs for Self Check Purposes

APPLICATIONS INFORMATION

SYSTEM LEVEL POWER MANAGEMENT

Transmit Level = 1.0 V pk-pk

For shorter reach applications supporting cable lengths up to 400 m, signal amplitude requirements tend to be lower, the Transmit mode of 1.0 V pk-pk can be used in such applications.

For applications where it is required that the ADIN1100 operates in a 1.0 V pk-pk transmit operating mode, the RXD_0/TX2P4_ENB pin must be tied high via a 4.7 kΩ resistor (see Figure 10). This configuration forces the ADIN1100 to operate at only 1.0 V pk-pk transmit operating mode and enables the operation of the ADIN1100 from a signal supply voltage operating at a lower voltage rail (e.g. 1.8 V), allowing the user to minimize power dissipation in the system. When this mode is selected, the CEXT_1 and CEXT_4 capacitors are not required.

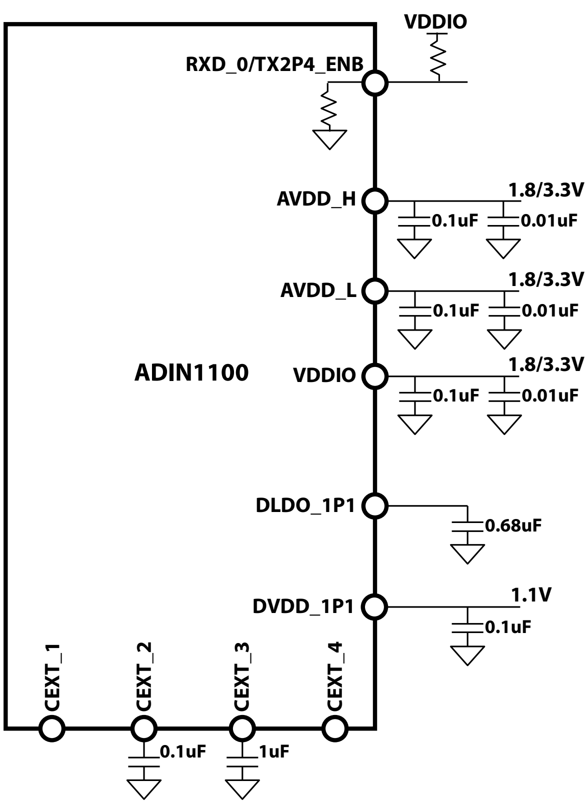


Figure 10. Supplies and capacitors for forced 1V pk-pk transmit mode

Transmit Level = 2.4 V pk-pk

For longer reach applications a higher signal amplitude of 2.4 V pk-pk is required. The ADIN1100 is designed to operate with long reach cables up to 1000 m in this mode requiring a higher AVDD_H supply voltage of 3.3 V.

For the ADIN1100 to be able to operate in 2.4 V pk-pk, the RXD_0/TX2P4_ENB pin must not be connected to the pull-up resistor. This mode of operation still allows the 1.0 V pk-pk operating mode to be selected via MDIO or via autonegotiation.

Figure 11 shows an overview of the proposed power configuration. Note that this configuration requires that AVDD_H is 3.3 V even if the link is established at 1.0 V pk-pk transmit operating mode via MDIO or autonegotiation. The CEXT_1 capacitor can be reduced to 2.2 µF in this configuration as long as it does not go below 2 µF over temperature, voltage, etc.

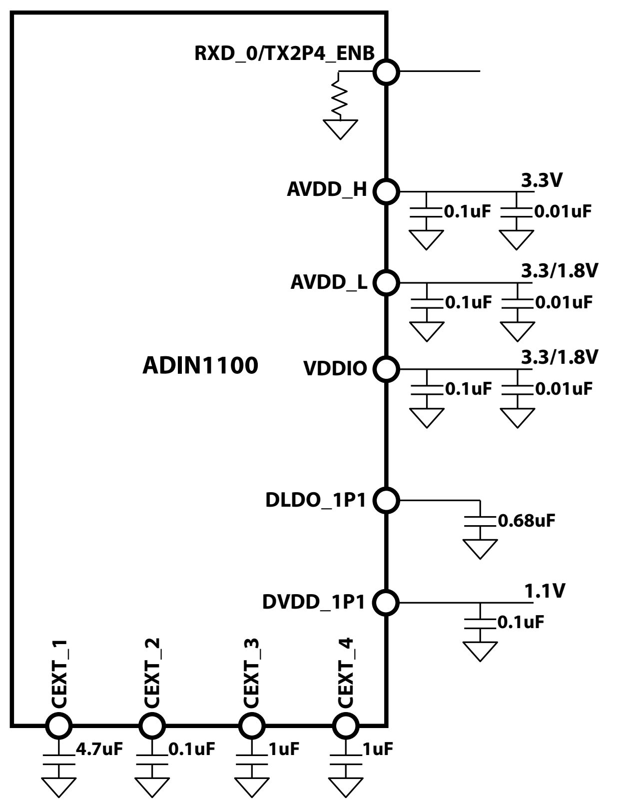


Figure 11. Supplies and capacitors for 2.4/1.0 V pk-pk transmit mode

For single supply operation, the same rail can be used to supply the ADIN1100 AVDD_H, AVDD_L and VDDIO supply rails. The DVDD_1P1 1.1 V rail can be derived internally or alternatively provided by an external 1.1 V rail. This configuration can be seen in Figure 12.

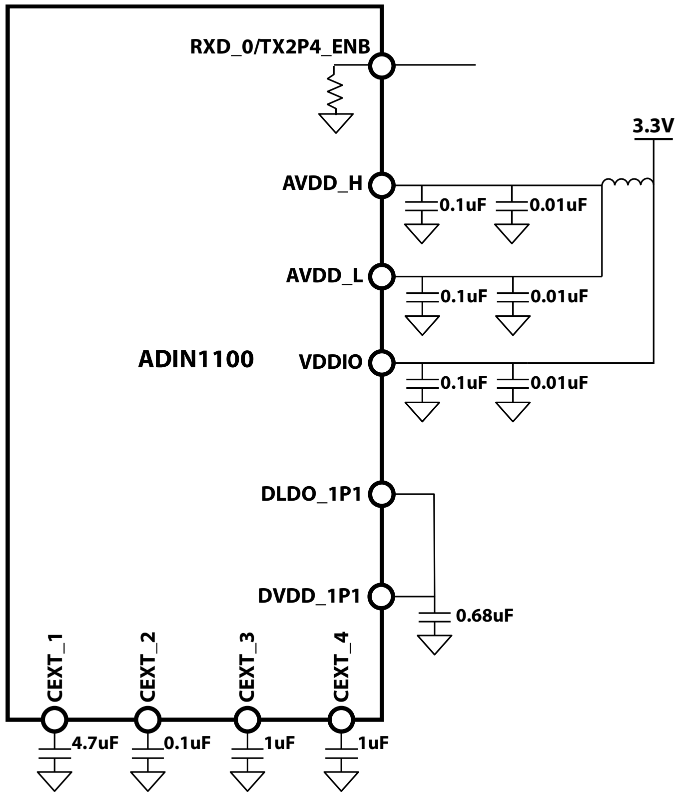


Figure 12. Supplies and capacitors for single supply 2.4 V pk-pk transmit mode

COMPONENT RECOMMENDATIONS

Crystal

The typical connection for an external crystal (XTAL) is shown in Figure 13. To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1100 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

The crystal specification defines C_L. Assuming the following:

- $C_{PCB1} \approx C_{PCB2} \approx C_{PCB}$
- $C_{X1} \approx C_{X2} \approx C_X$

Then, $C_X = 2 \times C_L - C_{PCB} - 3$ pF

Choose precision capacitors for C_X with low appreciable temperature coefficient to minimize frequency errors.

Ensure good ground connections on C_{X1}, C_{X2}, the package ground of the quartz resonator and the ground paddle of the ADIN1100 package.

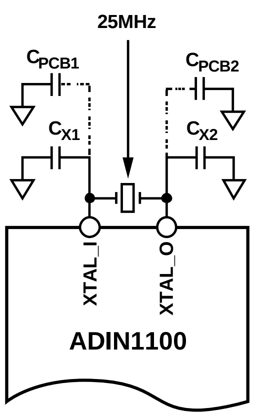


Figure 13. Crystal Oscillator Connection

External Clock Input

If using a single-ended reference clock on XTAL_I/CLK_IN, leave XTAL_O open-circuit. This clock must be an ac-coupled 0.8 V - 2.5 V pk-pk sine or (filtered) square wave signal. This also applies when connecting CLK25_REF output clock from one 10BASE-T1L device to the XTAL_I/CLK_IN input of another 10BASE-T1L device. When using the RMII MAC interface, a single, 50 MHz reference clock (REF_CLK) is required, which can be sourced from the MAC or from an external source.

If $V_{S\ pk\text{-}pk} < 2.5\ V_{pk\text{-}pk}$

- C_2 is not required
- C_1 = 1nF

If $V_{S\ pk\text{-}pk} \geq 2.5\ V_{pk\text{-}pk}$

- C_2 = 10 pF
- $C_1 = 2.5\ (13\text{pF} + C_{PCB}) / (V_{S\ pk\text{-}pk} - 2.5)$

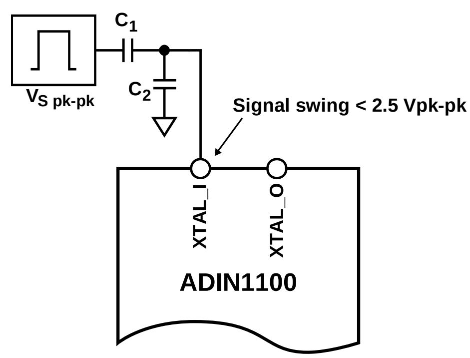


Figure 14. External Clock Connection

REGISTER SUMMARY

The MII management interface provides a 2-wire serial interface between a host processor or MAC and the ADIN1100 allowing access to control and status information in the management registers.

The interface is compatible with the IEEE Standard 802.3 Clause 45 management frame structure. The MDIO interface of the ADIN1100 cannot interface with the MDIO interfaces of microcontrollers that only support IEEE Standard 802.3 Clause 22. In these cases, the user can replicate the IEEE Standard 802.3 Clause 45 management frame structure with two of the microcontroller's GPIOs.

The registers are made up of four device address groupings (see Table 1) based on the MDIO Manageable Device (MMD). Within each device address space, IEEE standard registers are located in register addresses between 0x0000 and 0x7FFF and vendor specific registers are located in register addresses from 0x8000 to 0xFFFF.

Table 15. Register Groupings

Device Address	MMD Name
0x01	PMA/PMD (Physical Medium Attachment/Physical Medium Dependent)
0x03	PCS (Physical Coding Sublayer)
0x07	Auto-Negotiation
0x1E	Vendor Specific 1

This allows access to up to 32 PHYs consisting of up to 32 MMDs through a single MDIO interface. The IEEE Clause 45 MMD register access format is shown in Table 16 and Table 17.

First an address frame is sent to specify the device address and register address. A second frame is then sent to perform the read or write on the selected address from the first frame. The default value of some of the registers are determined by the value of the hardware configuration pins, which are read just after the RESET_N pin is de-asserted. In these cases, the reset value in the register table is listed as pin dependent. This allows the default operation of the ADIN1100 to be configured without having to write to it over the MDIO interface. This is useful in unmanaged applications, where the desired operation of the PHY is configured from the hardware configuration pins without any software intervention. For unmanaged applications, do not configure the PHY to enter software power-down after reset to ensure that the PHY immediately attempts to bring up links as configured by the other hardware configuration pins. In managed applications, software is available to configure the PHY via the management interface. In this case, it is possible to use the hardware configuration pins to configure the PHY to enter software power-down mode after reset, such that the PHY can be configured before linking is attempted.

The possible access permissions of the registers are:

- R/W: read/write
- R: read only
- R LL: read only, latch low
- R LH: read only, latch high
- R/W SC: read/write, self-clear

Table 16. Clause 45 Frame Format

MSB LSB

D31 to D30	D29 to D28	D27 to D23	D22 to D18	D17 to D16	D15 to D0
ST	OP	PHYADR	DEVAD	TA	Address/Data

Table 17. Input Register Decode

Bit	Description
ST	2 bit Start of Frame (00 for Clause 45)
OP	2 bit OP Code 00 - Address 01 - Write 11 - Read 10 – Read + Address
PHYADR	5 bit PHY Address
DEVAD	5 bit Device Address
TA	2 bit Turn Around field – used to avoid contention during a read transition, 2-bit time spacing between register address field and data field.
Address/Data	16 bit Register Address/Data

Recommended Register Operation

Many of the registers in the ADIN1100 are defined in the IEEE Standard 802.3 and the exact behavior of these registers follows the standard. This behavior may not always be obvious and is described here including the recommended operation and use of the registers.

Latch Low Registers

The IEEE Standard 802.3-2018 requires certain MDIO accessible registers to exhibit latch low behavior. The idea is to allow software that only intermittently reads these registers to detect conditions that may be transitory or short lived. For example, the AN_LINK_STATUS bit, is required to latch low. When the device exits from a reset or powerdown state, the latching condition is not active and the value of the AN_LINK_STATUS bit reflects the current status of the link. However, if the link comes up and subsequently drops, then the latching condition becomes active. In this case the AN_LINK_STATUS bit reads as 1'b0 even if the link has come back up again in the interim. The latching condition is only cleared once the AN_LINK_STATUS bit is read. This ensures that software has had the opportunity to observe that the link dropped.

One implication of the latch low behavior described above is that, if software wishes to determine the current status of the link, it must perform two reads of the AN_LINK_STATUS bit back-to-back. The first read is needed to clear any active latching condition.

Another implication is that it is important that software take account of the interaction between MDIO accessible bits that share a register address. For example, the AN_PAGE_RX and AN_LINK_STATUS bits reside at the same register address. As a result, reading the AN_PAGE_RX bit will clear any active latching condition associated with the AN_LINK_STATUS bit.

IEEE Duplicated Registers

The IEEE Standard 802.3-2018 covers a very wide range of standards and speeds from 10 Mb/s to 40 Gb/s and higher and includes a very large number of clauses. There are registers associated with many clauses and different PHYs may include different clauses and combinations of clauses. Hence, registers for common functions like software reset, software powerdown, loopback, etc. tend to be implemented in multiple clauses.

In the ADIN1100, the physical implementation of these registers is in a single location, but they may be accessed at multiple addresses. For example, the Software Reset bit, can be read or written in all the following IEEE MMD locations and vendor specific register locations:

- PMA_SFT_RST (device address 0x01, register address 0x0000, bit 15)
- B10L_PMA_SFT_RST (device address 0x01, register address 0x08F6, bit 15)
- PCS_SFT_RST (device address 0x3, register address 0x0000, bit 15)
- B10L_PCS_SFT_RST (device address 0x03, register address 0x08E6, bit 15)
- CRSM_SFT_RST (device address 0x1E, register address 0x8810, bit 15)

Note, in this example these are the PMA/PMD, PCS, Auto-Negotiation and Vendor Specific MMD 1 device address locations (per Table 15).

Having multiple address locations for the same register makes the use of the part more complex than necessary, in particular in relation to registers that have latch low or self-clear access permissions. Unfortunately, this is an unavoidable consequence of the IEEE standard.

The ADIN1100 datasheet only calls out a single recommended address location for each of these IEEE registers. This is done to simplify the operation and use of the part. In general, the registers introduced in the 802.3cg (10BASE-T1L) section of the standard are recommended over older (equivalent) registers. Often registers in a vendor specific address are recommended, in particular where a register brings a number of useful IEEE register bits into a single register address. The ADIN1100 will correctly respond to register accesses to all the IEEE register address locations covered by the 10BASE-T1L standard once the start-up is complete after power on reset, hardware reset or software reset.

Read Modify Write Operation

It is strongly recommended that all register write operations should be performed as read modify write operations. If this is not followed, it is possible that the value of register bits are inadvertently changed.

REGISTER DETAILS

Table 18. Register Summary

Device Address	Register Address	Name	Description	Reset	Access
0x01	0x0012	PMA_PMD_BT1_ABILITY	BASE-T1 PMA/PMD Extended Ability Register.	0x0004	R
0x01	0x0834	PMA_PMD_BT1_CONTROL	BASE-T1 PMA/PMD Control Register.	0x8002	R/W
0x01	0x08F6	B10L_PMA_CNTRL	10BASE-T1L PMA Control Register.	0x0000	R/W
0x01	0x08F7	B10L_PMA_STAT	10BASE-T1L PMA Status Register.	0x2000	R
0x01	0x08F8	B10L_TEST_MODE_CNTRL	10BASE-T1L Test Mode Control Register.	0x0000	R/W
0x01	0x8302	B10L_PMA_LINK_STAT	10BASE-T1L PMA Link Status Register.	0x0000	R
0x03	0x08E6	B10L_PCS_CNTRL	10BASE-T1L PCS Control Register.	0x0000	R/W
0x07	0x0200	AN_CONTROL	BASE-T1 Autonegotiation Control Register.	0x1000	R/W
0x07	0x0201	AN_STATUS	BASE-T1 Autonegotiation Status Register.	0x0008	R
0x07	0x0202	AN_ADV_ABILITY_L	BASE-T1 Autonegotiation Advertisement [15:0] Register.	0x0001	R/W
0x07	0x0203	AN_ADV_ABILITY_M	BASE-T1 Autonegotiation Advertisement [31:16] Register.	0x4000	R/W
0x07	0x0204	AN_ADV_ABILITY_H	BASE-T1 Autonegotiation Advertisement [47:32] Register.	0x0000	R/W
0x07	0x0205	AN_LP_ADV_ABILITY_L	BASE-T1 Autonegotiation Link Partner Base Page Ability [15:0] Register.	0x0000	R
0x07	0x0206	AN_LP_ADV_ABILITY_M	BASE-T1 Autonegotiation Link Partner Base Page Ability [31:16] Register.	0x0000	R
0x07	0x0207	AN_LP_ADV_ABILITY_H	BASE-T1 Autonegotiation Link Partner Base Page Ability [47:32] Register.	0x0000	R
0x07	0x0208	AN_NEXT_PAGE_L	BASE-T1 Autonegotiation Next Page Transmit [15:0] Register.	0x2001	R/W
0x07	0x0209	AN_NEXT_PAGE_M	BASE-T1 Autonegotiation Next Page Transmit [31:16] Register.	0x0000	R/W
0x07	0x020A	AN_NEXT_PAGE_H	BASE-T1 Autonegotiation Next Page Transmit [47:32] Register.	0x0000	R/W
0x07	0x020B	AN_LP_NEXT_PAGE_L	BASE-T1 Autonegotiation Link Partner Next Page Ability [15:0] Register.	0x0000	R
0x07	0x020C	AN_LP_NEXT_PAGE_M	BASE-T1 Autonegotiation Link Partner Next Page Ability [31:16] Register.	0x0000	R
0x07	0x020D	AN_LP_NEXT_PAGE_H	BASE-T1 Autonegotiation Link Partner Next Page Ability [47:32] Register.	0x0000	R
0x07	0x8001	AN_STATUS_EXTRA	Extra Autonegotiation Status Register.	0x0000	R
0x1E	0x0002	MMD1_DEV_ID1	Vendor Specific MMD 1 Device Identifier High Register.	0x0283	R
0x1E	0x0003	MMD1_DEV_ID2	Vendor Specific MMD 1 Device Identifier Low Register.	0xBC80	R
0x1E	0x0010	CRSM_IRQ_STATUS	System Interrupt Status Register.	0x0800	R
0x1E	0x0011	PHY_SUBSYS_IRQ_STATUS	PHY Subsystem Interrupt Status Register.	0x0000	R
0x1E	0x0020	CRSM_IRQ_MASK	System Interrupt Mask Register.	0x0FFF	R/W
0x1E	0x0021	PHY_SUBSYS_IRQ_MASK	PHY Subsystem Interrupt Mask Register.	0x2403	R/W
0x1E	0x8001	FC_EN	Frame Checker Enable Register.	0x0001	R/W
0x1E	0x8004	FC_IRQ_EN	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x1E	0x8005	FC_TX_SEL	Frame Checker Transmit Select Register.	0x0000	R/W
0x1E	0x8008	RX_ERR_CNT	Receive Error Count Register.	0x0000	R
0x1E	0x8009	FC_FRM_CNT_H	Frame Checker Count High Register.	0x0000	R
0x1E	0x800A	FC_FRM_CNT_L	Frame Checker Count Low Register.	0x0000	R
0x1E	0x800B	FC_LEN_ERR_CNT	Frame Checker Length Error Count Register.	0x0000	R
0x1E	0x800C	FC_ALGN_ERR_CNT	Frame Checker Alignment Error Count Register.	0x0000	R

Device Address	Register Address	Name	Description	Reset	Access
0x1E	0x800D	FC_SYMB_ERR_CNT	Frame Checker Symbol Error Count Register.	0x0000	R
0x1E	0x800E	FC_OSZ_CNT	Frame Checker Oversized Frame Count Register.	0x0000	R
0x1E	0x800F	FC_USZ_CNT	Frame Checker Undersized Frame Count Register.	0x0000	R
0x1E	0x8010	FC_ODD_CNT	Frame Checker Odd Nibble Frame Count Register.	0x0000	R
0x1E	0x8011	FC_ODD_PRE_CNT	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x1E	0x8013	FC_FALSE_CARRIER_CNT	Frame Checker False Carrier Count Register.	0x0000	R
0x1E	0x8015	FG_EN	Frame Generator Enable Register.	0x0000	R/W
0x1E	0x8016	FG_CNTRL_RSTRT	Frame Generator Control/Restart Register.	0x0001	R/W
0x1E	0x8017	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x1E	0x8018	FG_IRQ_EN	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x1E	0x801A	FG_FRM_LEN	Frame Generator Frame Length Register.	0x006B	R/W
0x1E	0x801C	FG_NFRM_H	Frame Generator Number of Frames High Register.	0x0000	R/W
0x1E	0x801D	FG_NFRM_L	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x1E	0x801E	FG_DONE	Frame Generator Done Register.	0x0000	R
0x1E	0x8038	RMII_CFG	RMII Configuration Register.	0x0006	R/W
0x1E	0x803D	MAC_IF_LOOPBACK	MAC Interface Loopbacks Configuration Register.	0x000A	R/W
0x1E	0x8810	CRSM_SFT_RST	Software Reset Register.	0x0000	R/W
0x1E	0x8812	CRSM_SFT_PD_CNTRL	Software Power-down Control Register.	0x0000	R/W
0x1E	0x8814	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset Register.	0x0000	R/W
0x1E	0x8815	CRSM_MAC_IF_RST	PHY MAC Interface Reset Register.	0x0000	R/W
0x1E	0x8818	CRSM_STAT	System Status Register.	0x0000	R
0x1E	0x882B	CRSM_MAC_IF_CFG	MAC Interface Configuration Register.	0x0000	R/W
0x1E	0x8C80	LED_BLINK_TIME_CNTRL	LED Blink Time Control Register.	0x0505	R/W
0x1E	0x8C81	LED_CNTRL	LED Control Register.	0x0000	R/W

BASE-T1 PMA/PMD Extended Ability Register

Device Address: 0x01; Register Address: 0x0012, Reset: 0x0004, Name: PMA_PMD_BT1_ABILITY

This address corresponds to the BASE-T1 PMA/PMD extended ability register specified in Clause 45.2.1.16 of Standard 802.3. This register is read only and writes have no effect.

Table 19. Bit Descriptions for PMA_PMD_BT1_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	B10S_ABILITY	10BASE-T1S Ability. This bit always reads as 1'b0 because the PMA/PMD does not support 10BASE-T1S.	0x0	R
2	B10L_ABILITY	10BASE-T1L Ability. This bit always reads as 1'b1 because the PMA/PMD supports 10BASE-T1L.	0x1	R
1	B1000_ABILITY	1000BASE-T1 Ability. This bit always reads as 1'b0 because the PMA/PMD does not support 1000BASE-T1.	0x0	R
0	B100_ABILITY	100BASE-T1 Ability. This bit always reads as 1'b0 because the PMA/PMD does not support 100BASE-T1.	0x0	R

BASE-T1 PMA/PMD Control Register

Device Address: 0x01; Register Address: 0x0834, Reset: 0x8002, Name: PMA_PMD_BT1_CONTROL

This address corresponds to the BASE-T1 PMA/PMD control register specified in Clause 45.2.1.185 of Standard 802.3.

Table 20. Bit Descriptions for PMA_PMD_BT1_CONTROL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x1	R
14	CFG_MST	Master-slave Config. CFG_MST is used only when autonegotiation is disabled; otherwise this value is determined by the autonegotiation process itself. When this bit is set as one, the part is configured as master. Otherwise, the part is configured as slave.	Pin Dependent	R/W
[13:4]	RESERVED	Reserved.	0x0	R
[3:0]	TYPE_SEL	Type Selection. This configuration is only used when autonegotiation is disabled. See IEEE Std 802.3 Table 45-149. Values other than those shown below should be considered reserved. 0010: 10BASE-T1L.	0x2	R/W

10BASE-T1L PMA Control Register

Device Address: 0x01; Register Address: 0x08F6, Reset: 0x0000, Name: B10L_PMA_CNTRL

This address corresponds to the 10BASE-T1L PMA control register specified in Clause 45.2.1.186a of Standard 802.3cg

Table 21. Bit Descriptions for B10L_PMA_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_TX_DIS_MODE_EN	10BASE-T1L Transmit Disable Mode. When this bit is set to one it disables output on the transmit path. Otherwise, it enables output on the transmit path.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
12	B10L_TX_LVL_HI	10BASE-T1L Transmit Voltage Amplitude Control. This configuration is only used when autonegotiation is disabled. Otherwise, the configuration is decided by the autonegotiation process. When this bit is set as one, the part works in the 2.4 V pk-pk operating mode. Otherwise, the part works in the 1.0 V pk-pk operating mode.	Pin Dependent	R/W
11	RESERVED	Reserved.	Pin Dependent	R/W
[10:1]	RESERVED	Reserved.	0x0	R/W
0	B10L_LB_PMA_LOC_EN	10BASE-T1L PMA Loopback. When this bit is set to one, the PMA accepts data on the transmit path and returns it on the receive path. When this bit is set to zero, the PMA works in normal mode.	0x0	R/W

10BASE-T1L PMA Status Register

Device Address: 0x01; Register Address: 0x08F7, Reset: 0x2000, Name: B10L_PMA_STAT

This address corresponds to the 10BASE-T1L PMA status register specified in Clause 45.2.1.186b of Standard 802.3cg

Table 22. Bit Descriptions for B10L_PMA_STAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	B10L_LB_PMA_LOC_ABLE	10BASE-T1L PMA Loopback Ability. This bit always reads as 1'b1 as the PMA has loopback ability	0x1	R
12	B10L_TX_LVL_HI_ABLE	10BASE-T1L High Voltage Tx Ability. Indicates that the PHY supports 10BASE-T1L high voltage (2.4 V pk-pk) transmit level operating mode.	Pin Dependent	R
[11:3]	RESERVED	Reserved.	0x0	R
2	B10L_POL_INV	10BASE-T1L Polarity Inverse. When this bit is read as a zero, it means that the polarity of the receiver is not reversed. When it is read as a one, it indicates that the polarity of the receiver is reversed.	0x0	R
[1:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L Test Mode Control Register

Device Address: 0x01; Register Address: 0x08F8, Reset: 0x0000, Name: B10L_TEST_MODE_CNTRL

This address corresponds to the 10BASE-T1L PMA test mode control register specified in Clause 45.2.1.186c of Standard 802.3cg. The default value of this register selects normal operation without management intervention as the initial state of the device.

Table 23. Bit Descriptions for B10L_TEST_MODE_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:13]	B10L_TX_TEST_MODE	10BASE-T1L Transmitter Test Mode. 000: Normal operation. 001: Test mode 1 - Transmitter output voltage and timing jitter test mode. When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, -1). 010: Test mode 2 - Transmitter output droop test mode. When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "-1" symbols. 011: Test mode 3 - Normal operation in Idle mode. When test mode 3 is enabled, the PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals.	0x0	R/W
[12:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PMA Link Status Register

Device Address: 0x01; Register Address: 0x8302, Reset: 0x0000, Name: B10L_PMA_LINK_STAT

This address may be read to determine the 10BASE-T1L PMA link status. Reading B10L_PMA_LINK_STAT clears the latching condition of these bits

Table 24. Bit Descriptions for B10L_PMA_LINK_STAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	B10L_REM_RCVR_STAT_OK_LL	10BASE-T1L Remote Receiver Status Ok Latch Low. Latched low version of B10L_REM_RCVR_STAT_OK.	0x0	R LL
12	B10L_REM_RCVR_STAT_OK	10BASE-T1L Remote Receiver Status Ok. When read as 1 this bit indicates that the remote receiver status is OK.	0x0	R
11	B10L_LOC_RCVR_STAT_OK_LL	10BASE-T1L Local Receiver Status Ok Latch Low. Latched low version of B10L_LOC_RCVR_STAT_OK.	0x0	R LL
10	B10L_LOC_RCVR_STAT_OK	10BASE-T1L Local Receiver Status Ok. When read as 1 this bit indicates that the local receiver status is OK.	0x0	R
9	B10L_DSCR_STAT_OK_LL	BASE-T1L Descrambler Status Ok Latch Low. When read as one this bit indicates that the descrambler status is OK.	0x0	R LL
8	B10L_DSCR_STAT_OK	10BASE-T1L Descrambler Status Ok. When read as 1 this bit indicates that the descrambler status is OK.	0x0	R
[7:2]	RESERVED	Reserved.	0x0	R
1	B10L_LINK_STAT_OK_LL	Link Status Ok Latch Low. When read as 1 this bit indicates that the link status is OK.	0x0	R LL
0	B10L_LINK_STAT_OK	Link Status OK. When read as 1 this bit indicates that the link status is OK.	0x0	R

10BASE-T1L PCS Control Register

Device Address: 0x03; Register Address: 0x08E6, Reset: 0x0000, Name: B10L_PCS_CNTRL

This address corresponds to the 10BASE-T1L PCS control register specified in Clause 45.2.3.68a of Standard 802.3cg.

Table 25. Bit Descriptions for B10L_PCS_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_LB_PCS_EN	PCS Loopback Enable. When set to one, this bit enables the 10BASE-T1L PCS loopback.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Control Register

Device Address: 0x07; Register Address: 0x0200, Reset: 0x1000, Name: AN_CONTROL

This address corresponds to the BASE-T1 autonegotiation control register specified in Clause 45.2.7.19 of Standard 802.3.

Table 26. Bit Descriptions for AN_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	AN_EN	Autonegotiation Enable. When this bit is set to one the Auto-Negotiation is enabled. Auto-Negotiation is enabled by default and it is strongly recommended that it is always enabled.	0x1	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	AN_RESTART	Autonegotiation Restart. Setting this bit to one restarts the autonegotiation process. This bit is self-clearing and it returns a value of one until the autonegotiation process has been initiated.	0x0	R/W SC
[8:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x0201, Reset: 0x0008, Name: AN_STATUS

This address corresponds to the BASE-T1 autonegotiation status register specified in Clause 45.2.7.20 of Standard 802.3.

Table 27. Bit Descriptions for AN_STATUS

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	AN_PAGE_RX	Page Received. This bit is set to indicate that a new link codeword has been received and stored in the AN_LP_ADV_ABILITY register or the AN_LP_NEXT_PAGE. The contents of the AN_LP_ADV_ABILITY are valid when this bit is set the first time during autonegotiation. This bit resets to zero on a read of the AN_STATUS register.	0x0	R LH
5	AN_COMPLETE	Autonegotiation Complete. When this bit is read as one, it means that the autonegotiation process has been completed, the PHY link is up, and that the contents of the AN_ADV_ABILITY and AN_LP_ADV_ABILITY are valid. This bit returns zero if the autonegotiation is disabled clearing the AN_EN bit.	0x0	R
4	RESERVED	Reserved.	0x0	R
3	AN_ABLE	Autonegotiation Ability. When this bit is read as one, it indicates that the PHY is able to perform autonegotiation.	0x1	R
2	AN_LINK_STATUS	Link Status. When read as one, this bit indicates that a valid link has been established. If this bit reads zero, it means that the link has failed since the last time it was read.	0x0	R LL
[1:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement [15:0] Register

Device Address: 0x07; Register Address: 0x0202, Reset: 0x0001, Name: AN_ADV_ABILITY_L

This address corresponds to the BASE-T1 autonegotiation advertisement register [15:0] specified in Clause 45.2.7.21 of Standard 802.3.

Table 28. Bit Descriptions for AN_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_ADV_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R/W
14	AN_ADV_ACK	Acknowledge (ACK). This bit indicates that the device has successfully received its link partner's link codeword. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_ADV_REMOTE_FAULT	Remote Fault. See IEEE Std 802.3 subclause 98.2.1.2.7.	0x0	R/W
12	AN_ADV_FORCE_MS	Force Master/slave Configuration. This bit allows the PHY to force its master/slave configuration. When this bit is set as zero, the master/slave configuration is a preferred mode (The configuration in AN_ADV_MST is a preferred configuration). If this bit is set to one, then the master/slave configuration is a forced mode (The configuration in AN_ADV_MST is a forced configuration) See IEEE Std 802.3 subclause 98.2.1.2.5 for more details.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[11:10]	AN_ADV_PAUSE	Pause Ability. This field advertises support for asymmetric and symmetric pause functions on full-duplex links. See IEEE Std 802.3 subclause 98.2.1.2.6 for more details.	0x0	R/W
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_ADV_SELECTOR	Selector. The value of this field is fixed at 5'b00001, which is the IEEE 802.3 selector value. See IEEE Std 802.3 subclause 98.2.1.2.1.	0x1	R

BASE-T1 Autonegotiation Advertisement [31:16] Register

Device Address: 0x07; Register Address: 0x0203, Reset: 0x4000, Name: AN_ADV_ABILITY_M

This address corresponds to the BASE-T1 autonegotiation advertisement register [31:16] specified in Clause 45.2.7.21 of Standard 802.3.

Table 29. Bit Descriptions for AN_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_ADV_B10L	10BASE-T1L Ability. This bit indicates that the device is compatible with 10BASE-T1L.	0x1	R/W
[13:5]	RESERVED	Reserved.	0x0	R
4	AN_ADV_MST	Master/slave Configuration. This bit advertises the master/slave configuration, as follows: 0: Slave 1: Master. See also AN_ADV_FORCE_MS register, which determines whether this bit expresses a preference or a forced value. See IEEE Std 802.3 subclause 98.2.1.2.3; Master/slave configuration is bit 4 of the Transmitted Nonce Field.	Pin Dependent	R/W
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement [47:32] Register

Device Address: 0x07; Register Address: 0x0204, Reset: 0x0000, Name: AN_ADV_ABILITY_H

This address corresponds to the BASE-T1 autonegotiation advertisement register [47:32] specified in Clause 45.2.7.21 of Standard 802.3.

Table 30. Bit Descriptions for AN_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	AN_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This bit advertises that the PHY is capable of transmitting in the high-level (2.4 V pk-pk) transmit operating mode. This bit is used with AN_ADV_B10L_TX_LVL_HI_REQ to configure 10BASE-T1L transmission level (2.4 V pk-pk or 1.0 V pk-pk); see the AN_ADV_B10L_TX_LVL_HI_REQ for more details.	Pin Dependent	R/W
12	AN_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This bit advertises that the PHY is requesting that high-level (2.4 V pk-pk) transmit operating mode is used. Note the transmit level is resolved as follows: If either PHY is not capable of high-level transmission (and has AN_ADV_B10L_TX_LVL_HI_ABL = 0), then both PHYs must use the low voltage (1.0 V pk-pk) transmit operating mode. Otherwise, if either PHY requests high-level transmission (and has AN_ADV_B10L_TX_LVL_HI_REQ = 1), then both PHYs must use the high voltage (2.4 V pk-pk) transmit operating mode. See IEEE P802.cg subclause 146.6.4 for more details.	Pin Dependent	R/W
[11:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability [15:0] Register

Device Address: 0x07; Register Address: 0x0205, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_L

This address corresponds to the link partner's BASE-T1 autonegotiation base page ability register [15:0] specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of registers AN_LP_ADV_ABILITY_M and AN_LP_ADV_ABILITY_H is latched when AN_LP_ADV_ABILITY_L is read.

Table 31. Bit Descriptions for AN_LP_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_ADV_NEXT_PAGE_REQ	Link Partner Next Page Request. This bit indicates that the link partner PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R
14	AN_LP_ADV_ACK	Link Partner Acknowledge (ACK). This bit indicates that the device has successfully received its link partner's link codeword. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_LP_ADV_REMOTE_FAULT	Link Partner Remote Fault. See IEEE Std 802.3 subclause 98.2.1.2.7.	0x0	R
12	AN_LP_ADV_FORCE_MS	Link Partner Force Master/slave Configuration. This bit reports the link partner's forced master/slave configuration, with values as follows: 0: Preferred mode (AN_LP_ADV_MSTR is a preferred configuration) 1: Forced mode (AN_LP_ADV_MSTR is a forced configuration) See IEEE Std 802.3 subclause 98.2.1.2.5 for more details.	0x0	R
[11:10]	AN_LP_ADV_PAUSE	Link Partner Pause Ability. This field reports the link partner's support for asymmetric and symmetric pause functions on full-duplex links. See IEEE Std 802.3 subclause 98.2.1.2.6 for more details.	0x0	R
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_LP_ADV_SELECTOR	Link Partner Selector. The value of this field should be 5'b00001, which is the IEEE 802.3 selector value. See IEEE Std 802.3 subclause 98.2.1.2.1.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability [31:16] Register

Device Address: 0x07; Register Address: 0x0206, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_M

This address corresponds to the link partner's BASE-T1 autonegotiation base page ability register [31:16] specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 32. Bit Descriptions for AN_LP_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L	Link Partner 10BASE-T1L Ability. This bit indicates if the link partner has 10BASE-T1L ability.	0x0	R
[13:8]	RESERVED	Reserved.	0x0	R
7	AN_LP_ADV_B1000	Link Partner 1000BASE-T1 Ability. This bit indicates if the link partner has 1000BASE-T1 ability.	0x0	R
6	AN_LP_ADV_B10S_FD	Link Partner 10BASE-T1S Full Duplex Ability. This bit indicates if the link partner has 10BASE-T1S ability.	0x0	R
5	AN_LP_ADV_B100	Link Partner 100BASE-T1 Ability. This bit indicates if the link partner has 100BASE-T1 ability.	0x0	R
4	AN_LP_ADV_MST	Link Partner Master/Slave Configuration. This bit reports the link partner's master/slave configuration, as follows: 0: Slave. 1: Master. See also AN_LP_ADV_FORCE_MS register, which determines whether this bit expresses a preference or a forced value. See IEEE Std 802.3 subclause 98.2.1.2.3; Master/slave configuration is bit 4 of the Transmitted Nonce Field.	0x0	R
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability [47:32] Register

Device Address: 0x07; Register Address: 0x0207, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_H

This address corresponds to the link partner's BASE-T1 autonegotiation base page ability register [47:32] specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 33. Bit Descriptions for AN_LP_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L_EEE	Link Partner 10BASE-T1L EEE Ability. This bit reports if the link partner is capable of using 10BASE-T1L energy efficient ethernet.	0x0	R
13	AN_LP_ADV_B10L_TX_LVL_HI_ABL	Link Partner 10BASE-T1L High Level Transmit Operating Mode Ability. This bit reports whether the link partner is capable of transmitting in the high level (2.4 V pk-pk) transmit operating mode. This bit is used with AN_LP_ADV_B10L_TX_LVL_HI_REQ to configure 10BASE-T1L transmission level (2.4 V pk-pk or 1.0 V pk-pk); see the AN_ADV_B10L_TX_LVL_HI_REQ for more details.	0x0	R
12	AN_LP_ADV_B10L_TX_LVL_HI_REQ	Link Partner 10BASE-T1L High Level Transmit Operating Mode Request. This bit reports whether the link partner is requesting that high level (2.4 V pk-pk) transmit operating mode is used. See the AN_ADV_B10L_TX_LVL_HI_REQ for more details.	0x0	R
11	AN_LP_ADV_B10S_HD	Link Partner 10BASE-T1S Half Duplex Ability. This bit reports if the link partner is capable of using 10BASE-T1S half-duplex.	0x0	R
[10:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Next Page Transmit [15:0] Register

Device Address: 0x07; Register Address: 0x0208, Reset: 0x2001, Name: AN_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation next page transmit register [15:0] specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represent a message page with the message code set to Null. AN_NEXT_PAGE_M and AN_NEXT_PAGE_H should be written before AN_NEXT_PAGE_L.

Table 34. Bit Descriptions for AN_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R/W
14	AN_NP_ACK	Next Page Acknowledge. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_NP_MESSAGE_PAGE	Next Page Encoding. Indicates encoding of next page, as follows: 0: Unformatted next page. 1: Message next page.	0x1	R/W
12	AN_NP_ACK2	Acknowledge 2. Indicates whether the PHY can comply with the message. See IEEE Std 802.3 subclause 28.2.3.4.6.	0x0	R/W
11	AN_NP_TOGGLE	Toggle Bit. The Toggle bit is used to synchronize pages between the PH_YS. This always read as 0 (the toggle bit is set automatically by the Arbitration state machine).	0x0	R
[10:0]	AN_NP_MESSAGE_CODE	Message/unformatted Code Field. For a message page (AN_NP_MESSAGE_PAGE = 1), the valid values are defined in IEEE Std 802.3 Table 45-329: 1: Null Message. 5: Organizationally Unique Identifier Tagged Message. 6: AN Device Identifier Tag Code.	0x1	R/W

BASE-T1 Autonegotiation Next Page Transmit [31:16] Register

Device Address: 0x07; Register Address: 0x0209, Reset: 0x0000, Name: AN_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation next page transmit register [31:16] specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represent a message page with the message code set to Null. AN_NEXT_PAGE_M and AN_NEXT_PAGE_H should be written before AN_NEXT_PAGE_L.

Table 35. Bit Descriptions for AN_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED1	Unformatted Code Field 1.	0x0	R/W

BASE-T1 Autonegotiation Next Page Transmit [47:32] Register

Device Address: 0x07; Register Address: 0x020A, Reset: 0x0000, Name: AN_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation next page transmit register [47:42] specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represent a message page with the message code set to Null. AN_NEXT_PAGE_M and AN_NEXT_PAGE_H should be written before AN_NEXT_PAGE_L.

Table 36. Bit Descriptions for AN_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED2	Unformatted Code Field 2.	0x0	R/W

BASE-T1 Autonegotiation Link Partner Next Page Ability [15:0] Register

Device Address: 0x07; Register Address: 0x020B, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register [15:0] specified in Clause 45.2.7.24 of Standard 802.3. The values of AN_LP_NEXT_PAGE_M and AN_LP_NEXT_PAGE_H are latched when this register is read.

Table 37. Bit Descriptions for AN_LP_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R
14	AN_LP_NP_ACK	Link Partner Next Page Acknowledge. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_LP_NP_MESSAGE_PAGE	Link Partner Next Page Encoding. Indicates encoding of link partner next page, as follows: 0: Unformatted next page. 1: Message next page.	0x0	R
12	AN_LP_NP_ACK2	Link Partner Acknowledge 2. See AN_NP_ACK2 for more details.	0x0	R
11	AN_LP_NP_TOGGLE	Link Partner Toggle Bit. Link partner Toggle bit.	0x0	R
[10:0]	AN_LP_NP_MESSAGE_CODE	Link Partner Message/unformatted Code Field. See AN_NP_MESSAGE_PAGE for more details. 1: Null Message. 5: Organizationally Unique Identifier Tagged Message. 6: AN Device Identifier Tag Code.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability [31:16] Register

Device Address: 0x07; Register Address: 0x020C, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register [31:16] specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 38. Bit Descriptions for AN_LP_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED1	Link Partner Unformatted Code Field 1.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability [47:32] Register

Device Address: 0x07; Register Address: 0x020D, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register [47:32] specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 39. Bit Descriptions for AN_LP_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED2	Link Partner Unformatted Code Field 2.	0x0	R

Extra Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x8001, Reset: 0x0000, Name: AN_STATUS_EXTRA

Provided in addition to AN_STATUS

Table 40. Bit Descriptions for AN_STATUS_EXTRA

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
8	AN_LP_NP_RX	Next Page Request Received from Link Partner.	0x0	R LH
7	AN_INC_LINK	Incompatible Link Indication. This corresponds to the state incompatible_link of IEEE Std 802.3 subclause 98.5.1. Its value is set by the Priority Resolution function run on entering the AN GOOD CHECK state.	0x0	R
[6:5]	AN_MS_CONFIG_RSLTN	Master/slave Resolution Result. Determined as per Table 98-4 - master-slave Configuration of IEEE Std 802.3. This is encoded as follows: 0: Not run. 1: Configuration fault. 2: Success, PHY is configured as SLAVE. 3: Success, PHY is configured as MASTER.	0x0	R
[4:1]	AN_HCD_TECH	Highest Common Denominator (HCD) PHY Technology. As selected by the Priority Resolution function of IEEE Std 802.3 subclause 98.2.4.2. Values other than those shown below should be considered reserved. 0: NULL (not run). 1: 10BASE-T1L.	0x0	R
0	AN_LINK_GOOD	Autonegotiation Complete Indication. This corresponds to the state an_link_good of IEEE Std 802.3 subclause 98.5.1. This signal indicates completion of the autonegotiation transmission, and that the enabled PHY technology is either bringing up its link, or that it has brought up its link. See also AN_COMPLETE, which is similar, but also indicates that PHY link is up.	0x0	R

Vendor Specific MMD 1 Device Identifier High Register

Device Address: 0x1E; Register Address: 0x0002, Reset: 0x0283, Name: MMD1_DEV_ID1

This address corresponds to the vendor specific MMD 1 device identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows 16 bits of the organizationally unique identifier (OUI) to be observed.

Table 41. Bit Descriptions for MMD1_DEV_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEV_ID1	Organizationally Unique Identifier. Bits[3:18]	0x283	R

Vendor Specific MMD 1 Device Identifier Low Register

Device Address: 0x1E; Register Address: 0x0003, Reset: 0xBC80, Name: MMD1_DEV_ID2

This address corresponds to the vendor specific MMD 1 device identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows 6 bits of the OUI along with the model number and revision number to be observed.

Table 42. Bit Descriptions for MMD1_DEV_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MMD1_DEV_ID2_OUI	Organizationally Unique Identifier. Bits[19:24]	0x2F	R
[9:4]	MMD1_MODEL_NUM	Model Number.	0x8	R
[3:0]	MMD1_REV_NUM	Revision Number.	0x0	R

System Interrupt Status Register

Device Address: 0x1E; Register Address: 0x0010, Reset: 0x0800, Name: CRSM_IRQ_STATUS

This address may be used to check which interrupt requests have been triggered since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of CRSM_IRQ_STATUS go high even when the associated interrupts are not enabled. A reserved interrupt being triggered indicates a fatal error in the system.

Table 43. Bit Descriptions for CRSM_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_LH	Software Requested Interrupt Event.	0x0	R LH
[14:12]	RESERVED	Reserved.	0x0	R
11	CRSM_HRD_RST_IRQ_LH	Hardware Reset Interrupt.	0x1	R LH
[10:0]	RESERVED	Reserved.	0x0	R LH

PHY Subsystem Interrupt Status Register

Device Address: 0x1E; Register Address: 0x0011, Reset: 0x0000, Name: PHY_SUBSYS_IRQ_STATUS

This address may be read to check which interrupt events have occurred since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of PHY_SUBSYS_IRQ_STATUS go high even when the associated bits in PHY_SUBSYS_IRQ_MASK are not set. A reserved interrupt being triggered indicates a fatal error in the system.

Table 44. Bit Descriptions for PHY_SUBSYS_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R LH
14	MAC_IF_FC_FG_IRQ_LH	Mac Interface Frame Checker/Generator Interrupt.	0x0	R LH
13	MAC_IF_EBUF_ERR_IRQ_LH	Mac Interface Buffers Overflow/underflow Interrupt.	0x0	R LH
12	RESERVED	Reserved.	0x0	R LH
11	AN_STAT_CHNG_IRQ_LH	Autonegotiation Status Change Interrupt.	0x0	R LH
[10:2]	RESERVED	Reserved.	0x0	R LH
1	LINK_STAT_CHNG_LH	Link Status Change.	0x0	R LH
0	RESERVED	Reserved.	0x0	R LH

System Interrupt Mask Register

Device Address: 0x1E; Register Address: 0x0020, Reset: 0x0FFF, Name: CRSM_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 45. Bit Descriptions for CRSM_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_REQ	Software Interrupt Request. Software can set this bit to generate an interrupt for system level testing. This bit always reads as zero as it is self-clearing.	0x0	R/W SC
[14:12]	RESERVED	Reserved.	0x0	R
11	CRSM_HRD_RST_IRQ_EN	Enable Hardware Reset Interrupt. Note that writing a 0 to this register does not mask the interrupt since this register is initialized when a hardware reset occurs.	0x1	R/W
[10:0]	RESERVED	Reserved.	0x7FF	R/W

PHY Subsystem Interrupt Mask Register

Device Address: 0x1E; Register Address: 0x0021, Reset: 0x2403, Name: PHY_SUBSYS_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 46. Bit Descriptions for PHY_SUBSYS_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	MAC_IF_FC_FG_IRQ_EN	Enable Mac Interface Frame Checker/Generator Interrupt.	0x0	R/W
13	MAC_IF_EBUF_ERR_IRQ_EN	Enable Mac Interface Buffers Overflow/underflow Interrupt.	0x1	R/W
12	RESERVED	Reserved.	0x0	R/W
11	AN_STAT_CHNG_IRQ_EN	Enable Autonegotiation Status Change Interrupt.	0x0	R/W
[10:2]	RESERVED	Reserved.	0x100	R/W
1	LINK_STAT_CHNG_IRQ_EN	Enable Link Status Change Interrupt.	0x1	R/W
0	RESERVED	Reserved.	0x1	R/W

Frame Checker Enable Register

Device Address: 0x1E; Register Address: 0x8001, Reset: 0x0001, Name: FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the FC_TX_SEL register) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 47. Bit Descriptions for FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_EN	Frame Checker Enable. Set to 1'b1 to enable the frame checker	0x1	R/W

Frame Checker Interrupt Enable Register

Device Address: 0x1E; Register Address: 0x8004, Reset: 0x0001, Name: FC_IRQ_EN

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register.

Table 48. Bit Descriptions for FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_IRQ_EN	Frame Checker Interrupt Enable. When set, this bit enables the frame checker interrupt.	0x1	R/W

Frame Checker Transmit Select Register

Device Address: 0x1E; Register Address: 0x8005, Reset: 0x0000, Name: FC_TX_SEL

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received from the MAC interface to be transmitted are checked. The frame checker can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (see the MAC_IF_REM_LB_EN bit in the MAC_IF_LOOPBACK register) because it can be used to check the received data after it is looped back at the MAC interface.

Table 49. Bit Descriptions for FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_TX_SEL	Frame Checker Transmit Select. When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

Receive Error Count Register

Device Address: 0x1E; Register Address: 0x8008, Reset: 0x0000, Name: RX_ERR_CNT

The receive error counter register is used to access the receive error counter associated with the frame checker in the PHY

Table 50. Bit Descriptions for RX_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	RX_ERR_CNT	Receive Error Count. This is the receive error counter associated with the frame checker in the PHY. Note that this bit is self clearing upon reading.	0x0	R SC

Frame Checker Count High Register

Device Address: 0x1E; Register Address: 0x8009, Reset: 0x0000, Name: FC_FRM_CNT_H

This register is a latched copy of Bits [31:16] of the 32-bit of the receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and the receive frame count are synchronized.

Table 51. Bit Descriptions for FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_H	Bits [31:16] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Count Low Register

Device Address: 0x1E; Register Address: 0x800A, Reset: 0x0000, Name: FC_FRM_CNT_L

This register is a latched copy of Bits [15:0] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and receive frame count are synchronized.

Table 52. Bit Descriptions for FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_L	Bits [15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Length Error Count Register

Device Address: 0x1E; Register Address: 0x800B, Reset: 0x0000, Name: FC_LEN_ERR_CNT

This register is a latched copy of the frame length error counter register. This register is a count of received frames with a length error status. When the receive error counter (RX_ERR_CNT) is read, the frame length error counter register is latched, which ensures that the frame length error count and receive frame count are synchronized

Table 53. Bit Descriptions for FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter.	0x0	R

Frame Checker Alignment Error Count Register

Device Address: 0x1E; Register Address: 0x800C, Reset: 0x0000, Name: FC_ALGN_ERR_CNT

This register is a latched copy of the frame alignment error counter register. This register is a count of received frames with an alignment error status. When the receive error counter (RX_ERR_CNT) is read, the alignment error counter is latched, which ensures that the frame alignment error count and the receive frame count are synchronized.

Table 54. Bit Descriptions for FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Count Register

Device Address: 0x1E; Register Address: 0x800D, Reset: 0x0000, Name: FC_SYMB_ERR_CNT

This register is a latched copy of the symbol error counter register. This register is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RX_ERR_CNT) is read, the symbol error count is latched, which ensures that the symbol error count and the frame receive count are synchronized.

Table 55. Bit Descriptions for FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_SYMB_ERR_CNT	Latched Copy of the Symbol Error Counter.	0x0	R

Frame Checker Oversized Frame Count Register

Device Address: 0x1E; Register Address: 0x800E, Reset: 0x0000, Name: FC_OSZ_CNT

This register is a latched copy of the oversized frame error counter register. This register is a count of receiver frames with a length greater than specified in frame checker maximum frame size (FC_MAX_FRM_SIZE). When the receive error counter (RX_ERR_CNT) is read, the oversized frame counter register is latched, which ensures that the oversized error count and the receive frame count are synchronized.

Table 56. Bit Descriptions for FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_OSZ_CNT	Latched copy of the Overisized Frame Error Counter.	0x0	R

Frame Checker Undersized Frame Count Register

Device Address: 0x1E; Register Address: 0x800F, Reset: 0x0000, Name: FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with less than 64 bytes. When the receive error counter (RX_ERR_CNT) is read, the undersized frame error counter is latched, which ensures that the undersized frame error count and the receive frame count are synchronized.

Table 57. Bit Descriptions for FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter.	0x0	R

Frame Checker Odd Nibble Frame Count Register

Device Address: 0x1E; Register Address: 0x8010, Reset: 0x0000, Name: FC_ODD_CNT

This register is a latched copy of the odd nibble frame register. This register is a count of received frames with an odd number of frames in the frame. When the receive error counter (RX_ERR_CNT) is read, the odd nibble frame counter register is latched, which ensures that the odd nibble frame count and the receive frame count are synchronized.

Table 58. Bit Descriptions for FC_ODD_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_CNT	Latched Copy of the Odd Nibble Counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Device Address: 0x1E; Register Address: 0x8011, Reset: 0x0000, Name: FC_ODD_PRE_CNT

This register is a latched copy of the odd preamble packet counter register. This register is a count of received packets with an odd number of nibbles in the preamble. When the receive error counter (RX_ERR_CNT) is read, the odd preamble packet counter register is latched, which ensures that the odd preamble packet count and the receive frame count are synchronized.

Table 59. Bit Descriptions for FC_ODD_PRE_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_PRE_CNT	Latched Copy of the Odd Preamble Packet Counter.	0x0	R

Frame Checker False Carrier Count Register

Device Address: 0x1E; Register Address: 0x8013, Reset: 0x0000, Name: FC_FALSE_CARRIER_CNT

This register is a latched copy of the false carrier events counter register. This is a count of the number of times the BAD SSD state is entered. When the receive error counter (RX_CNT_ERR) is read, the false carrier events counter register is latched, which ensures that the false carrier events count and the receive frame count are synchronized.

Table 60. Bit Descriptions for FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

Frame Generator Enable Register

Device Address: 0x1E; Register Address: 0x8015, Reset: 0x0000, Name: FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled (DIAG_CLK_EN)

Table 61. Bit Descriptions for FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_EN	Frame Generator Enable.	0x0	R/W

Frame Generator Control/Restart Register

Device Address: 0x1E; Register Address: 0x8016, Reset: 0x0001, Name: FG_CNTRL_RSTRT

This register controls the frame generator. The FG_CNTRL bitfield specifies data field type used by the frame generator, e.g. random, all zeros, etc. The FG_RSTRT bit restarts the frame generator.

Table 62. Bit Descriptions for FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FG_RSTRT	Frame Generator Restart. When set, this bit restarts the frame generator. This bit is self-clearing	0x0	R/W SC
[2:0]	FG_CNTRL	Frame Generator Control. 000: No frames after completion of current frame 001: Random number data frame 010: All zeros data frame 011: All ones data frame 100: Alternative 0x55 data field 101: Data field decrementing from 255 (decimal) to 0	0x1	R/W

Frame Generator Continuous Mode Enable Register

Device Address: 0x1E; Register Address: 0x8017, Reset: 0x0000, Name: FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FG_NFRM_H and FG_NFRM_L registers.

Table 63. Bit Descriptions for FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_CONT_MODE_EN	This bit is used to put the frame generator into continuous mode or burst mode. 1: Frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: Frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames is determined by the FG_NFRM_H and FG_NFRM_L registers.	0x0	R/W

Frame Generator Interrupt Enable Register

Device Address: 0x1E; Register Address: 0x8018, Reset: 0x0000, Name: FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The interrupt status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register

Table 64. Bit Descriptions for FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_IRQ_EN	Frame Generator Interrupt Enable. When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

Frame Generator Frame Length Register

Device Address: 0x1E; Register Address: 0x801A, Reset: 0x006B, Name: FG_FRM_LEN

This register specifies the data field frame length in bytes. In addition to the data field, 6 bytes are added for the source address, 6 bytes for the destination address, 2 bytes for the length field, and 4 bytes for the frame check sequence (FCS). The total length is the data field length plus 18.

Table 65. Bit Descriptions for FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

Frame Generator Number of Frames High Register

Device Address: 0x1E; Register Address: 0x801C, Reset: 0x0000, Name: FG_NFRM_H

This register is Bits [31:16] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 66. Bit Descriptions for FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_H	Bits [31:16] of the Number of Frames to be Generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Device Address: 0x1E; Register Address: 0x801D, Reset: 0x0100, Name: FG_NFRM_L

This register is Bits [15:0] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 67. Bit Descriptions for FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_L	Bits [15:0] of the Number of Frames to be Generated.	0x100	R/W

Frame Generator Done Register

Device Address: 0x1E; Register Address: 0x801E, Reset: 0x0000, Name: FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FG_NFRM_H and FG_NFRM_L registers.

Table 68. Bit Descriptions for FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_DONE	Frame Generator Done. This bit reads as 1'b1 to indicate that the generation of frames has completed. When set, this bit goes high and it latches high until its unlatched by reading.	0x0	R LH

RMII Configuration Register

Device Address: 0x1E; Register Address: 0x8038, Reset: 0x0006, Name: RMII_CFG

Table 69. Bit Descriptions for RMII_CFG

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x3	R
0	RMII_TXD_CHK_EN	RMII TXD Check Enable. This bit determines whether or not TXD[1:0] is monitored to detect the start of a frame. It allows connecting the RMII Rx CRS_DV to the RMII TX_EN signal. It is mainly intended for debug and test purposes.	0x0	R/W

MAC Interface Loopbacks Configuration Register

Device Address: 0x1E; Register Address: 0x803D, Reset: 0x000A, Name: MAC_IF_LOOPBACK

MAC interface loopbacks configuration

Table 70. Bit Descriptions for MAC_IF_LOOPBACK

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	MAC_IF_REM_LB_RX_SUP_EN	Suppress RX Enable. Suppress RX to the MAC when MAC_IF_REM_LB_EN is set	0x1	R/W
2	MAC_IF_REM_LB_EN	MAC Interface Remote Loopback Enable. RX data is looped back to TX	0x0	R/W
1	MAC_IF_LB_TX_SUP_EN	Suppress Transmission Enable. Suppress transmission to the PHY when MAC_IF_LB_EN is set	0x1	R/W
0	MAC_IF_LB_EN	MAC Interface Loopback Enable. TX data is looped back to RX	0x0	R/W

Software Reset Register

Device Address: 0x1E; Register Address: 0x8810, Reset: 0x0000, Name: CRSM_SFT_RST

Table 71. Bit Descriptions for CRSM_SFT_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_RST	Software Reset Register. The software reset bit allows the chip to be reset. When this bit is set, a full initialization of the chip, almost equivalent to a hardware reset, is done.	0x0	R/W SC

Software Power-down Control Register

Device Address: 0x1E; Register Address: 0x8812, Reset: 0x0000, Name: CRSM_SFT_PD_CNTRL

Table 72. Bit Descriptions for CRSM_SFT_PD_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_PD	Software Power-down. The software power-down register puts the chip in a lower power mode. In this mode most of the circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this register is configurable via a pin. This allows the chip to be held in power-down mode until an appropriate software initialization has been performed.	Pin Dependent	R/W

PHY Subsystem Reset Register

Device Address: 0x1E; Register Address: 0x8814, Reset: 0x0000, Name: CRSM_PHY_SUBSYS_RST

Table 73. Bit Descriptions for CRSM_PHY_SUBSYS_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset. The PHY subsystem reset register allows a managed subsystem reset to be initiated. When the PHY subsystem is reset, normal operation resumes, and the bit is self-cleared.	0x0	R/W SC

PHY MAC Interface Reset Register

Device Address: 0x1E; Register Address: 0x8815, Reset: 0x0000, Name: CRSM_MAC_IF_RST

Table 74. Bit Descriptions for CRSM_MAC_IF_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_MAC_IF_RST	PHY MAC Interface Reset. The PHY MAC interface reset register allows a managed PHY MAC interface reset to be initiated. When the PHY MAC interface is reset, normal operation resumes, and the bit is self-cleared.	0x0	R/W SC

System Status Register

Device Address: 0x1E; Register Address: 0x8818, Reset: 0x0000, Name: CRSM_STAT

Table 75. Bit Descriptions for CRSM_STAT

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	CRSM_SFT_PD_RDY	Software Power-down Status. This bit indicates that the system is in the software power-down state.	0x0	R
0	CRSM_SYS_RDY	System Ready. This bit indicates that the start-up sequence is complete and the system is ready for normal operation.	0x0	R

MAC Interface Configuration Register

Device Address: 0x1E; Register Address: 0x882B, Reset: 0x0000, Name: CRSM_MAC_IF_CFG

Table 76. Bit Descriptions for CRSM_MAC_IF_CFG

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	Pin Dependent	R/W
[13:9]	RESERVED	Reserved.	0x0	R
8	CRSM_RMII_MEDIA_CNV_EN	Media Converter Enable. When this bit is 1, the media converter functionality for the RMII MAC interface mode is enabled. Note that the media convertor functionality can only be enabled if a RMII MAC interface is being used.	Pin Dependent	R/W
[7:5]	RESERVED	Reserved.	0x0	R
4	RESERVED	Reserved.	Pin Dependent	R/W
[3:1]	RESERVED	Reserved.	0x0	R
0	RESERVED	Reserved.	Pin Dependent	R/W

LED Blink Time Control Register

Device Address: 0x1E; Register Address: 0x8C80, Reset: 0x0505, Name: LED_BLINK_TIME_CNTRL

LED on/off blink time in number of ms x 4

Table 77. Bit Descriptions for LED_BLINK_TIME_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	LED_ON_N4MS	LED on Blink Time. This bitfield sets the LED on time to the value of the bitfield times 4 ms. For example, the value of 0x05 corresponds to 20 ms.	0x5	R/W
[7:0]	LED_OFF_N4MS	LED off Blink Time. This bitfield sets the LED off time to the value of the bitfield times 4 ms. For example, the value of 0x05 corresponds to 20 ms.	0x5	R/W

LED Control Register

Device Address: 0x1E; Register Address: 0x8C81, Reset: 0x0000, Name: LED_CNTRL

LED control register

Table 78. Bit Descriptions for LED_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	LED_EN	LED Enable. When this bit is 1'b1 the LED is enabled. Otherwise, the LED is disabled.	0x0	R/W

PCB LAYOUT RECOMMENDATIONS

This is an overview of the key areas of interest during placement and layout of the PHY and corresponding support components.

PHY PACKAGE LAYOUT

The LFCSP has an exposed pad underneath the package that must be soldered to the PCB ground for mechanical, electrical and thermal reasons. For thermal impedance performance and to maximize heat removal, use of a 4 × 4 array of thermal vias beneath the exposed ground pad is recommended. The PCB land pattern must incorporate the exposed ground paddle with these vias in the footprint. The EVAL-ADIN1100FMCZ uses an array of 4 × 4 filled vias on a 1.00 mm grid arrangement. The via pad diameter dimension is 0.02 in. (0.5015 mm).

COMPONENT PLACEMENT

Prioritization of the critical traces and components helps simplify the routing exercise. Place and orient the critical traces and components first to ensure an effective layout with minimal turns, vias, and crossing traces. For an 10BASE-T1L PHY layout, the important components are the crystal and load capacitors, the CEXT_1, CEXT_2, CEXT_3 and CEXT_4 capacitors as well as all bypass capacitors local to the ADIN1100 device. Prioritize these components and the routing to them. Keeping the MDI traces (RXP, RXN, TXP and TXN) closest to the ADIN100 as short as possible is also important.

Crystal Placement and Routing

To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1100 as possible.

OUTLINE DIMENSIONS

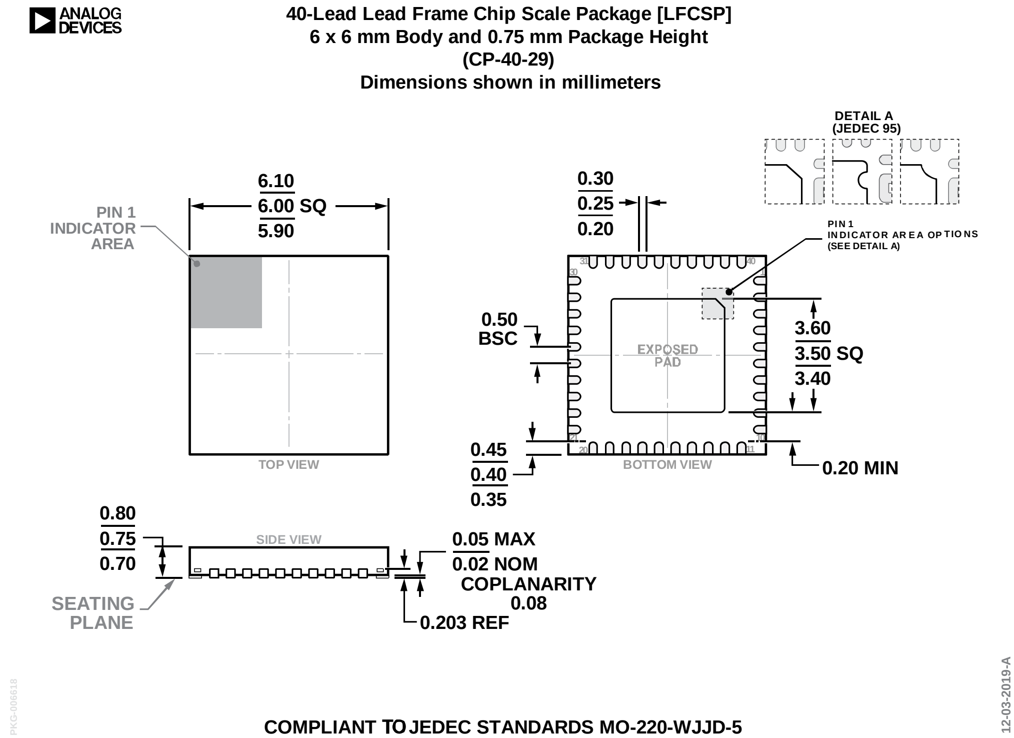


Figure 15. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm x 6 mm Body and 0.75 mm Package Height
(CP-40-29).
Dimensions shown in millimeters